

# Compal Confidential

## Hasswell M/B Schematics Document

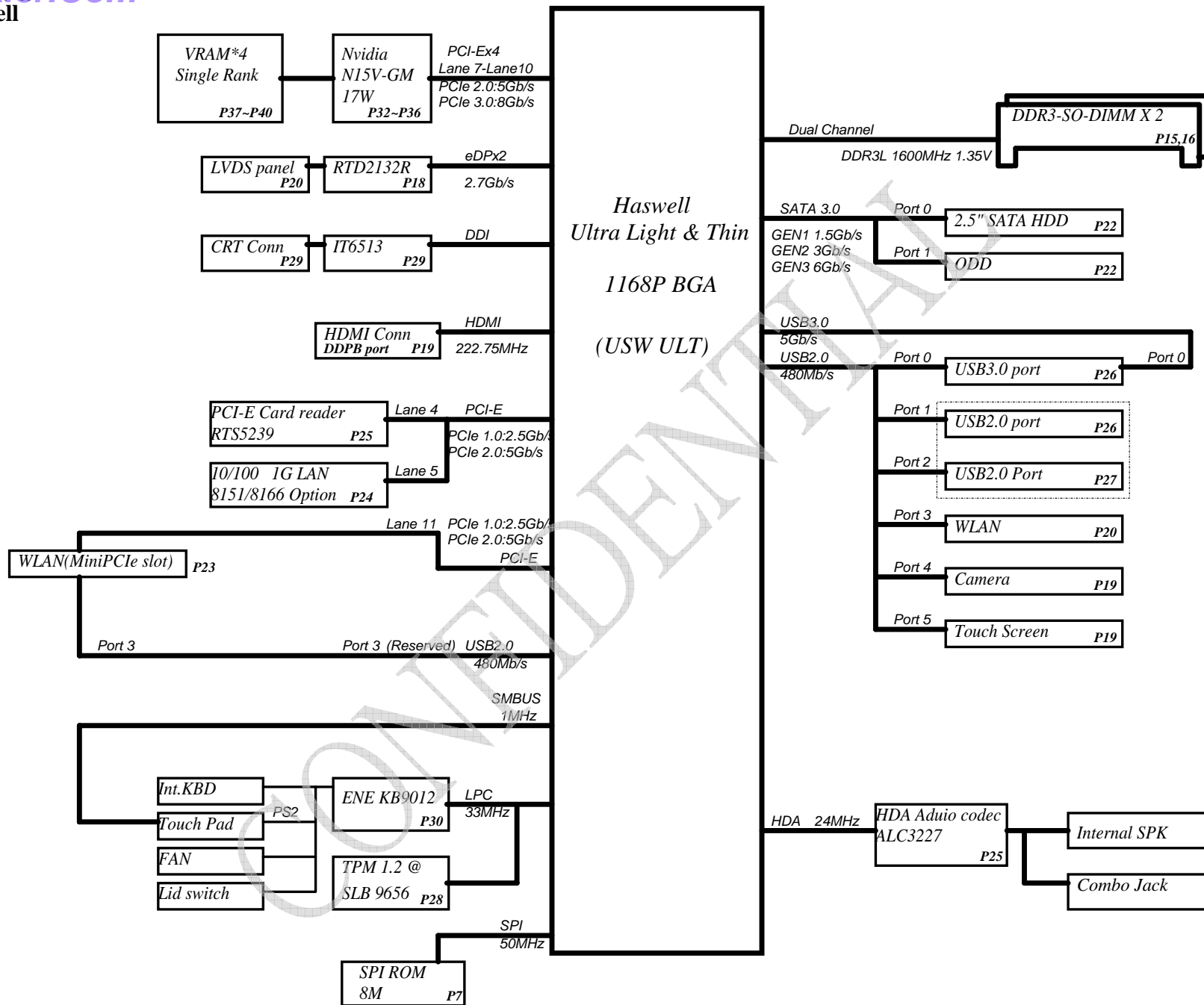
Intel ULV Processor with DDRIII

Date : 2014/02/08

Version 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Cover Page
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File Name :  
LA-A992PR10



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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.35V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.675VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)

short@ : short pad , don't pop.

@EMI@,@ESD@,@RF@ : Reserve , don't pop.

RF@ : RF team request, must add.

EMI@ : EMI team request, must add.

ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel.

GCLK@ : Support GCLK

CRT@,CRTEMI@ : Support CRT port

eDP@,eDPEMI@ : Support eTP panel

DAX  
PCB «BOM Structure»  
Part Number = DA214200100  
PCB 14Z LA-A992P REV0 M/B 3

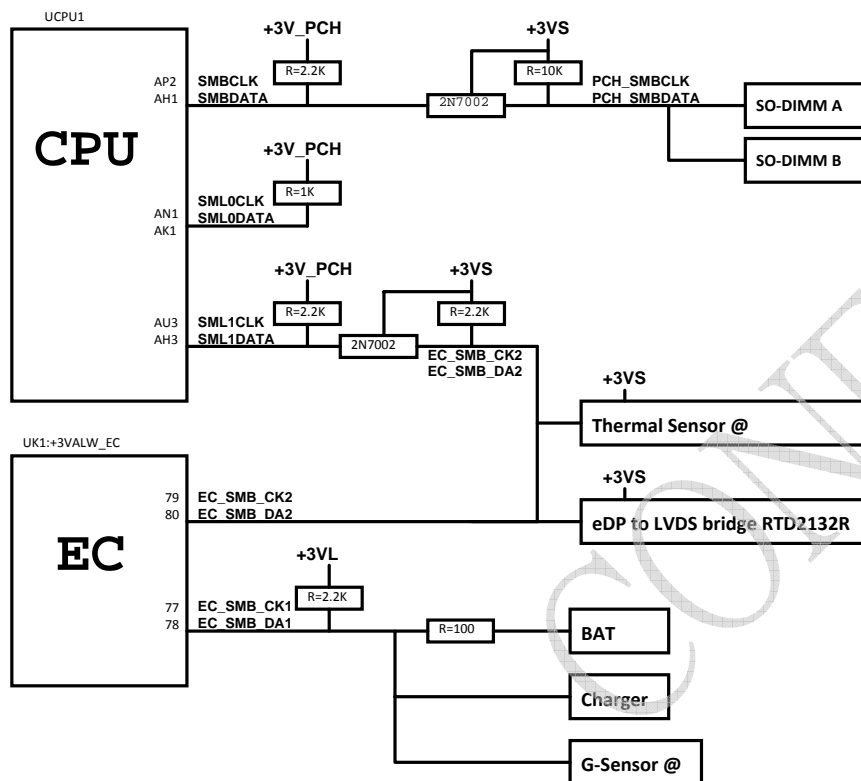
45@  
ZZZ1  
ROYALTY HDMI W/LOGO+HDCP  
Part Number = RO0000003HM  
ROYALTY HDMI W/LOGO+HDCP

### <USB2.0 port>

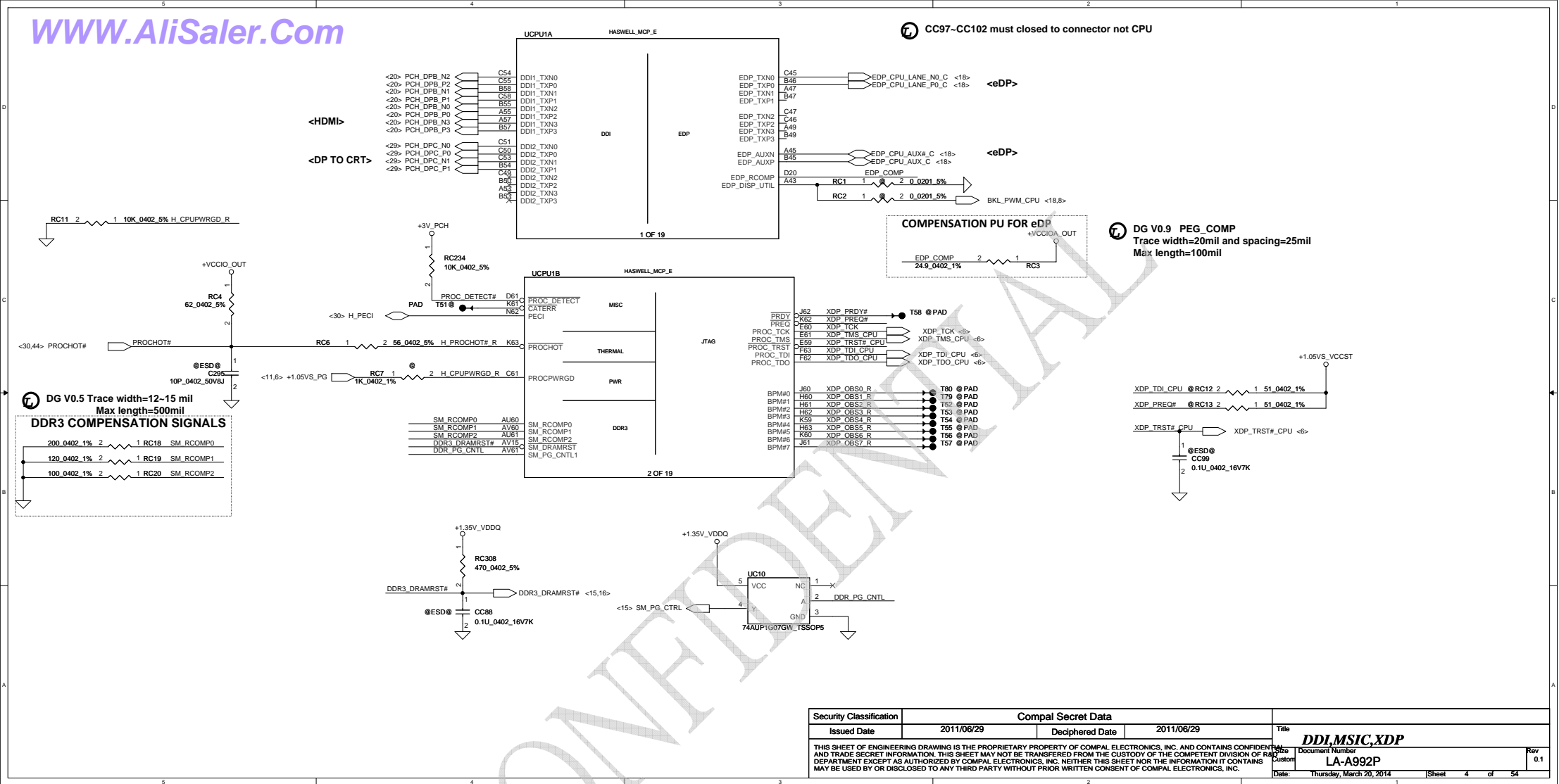
USB2.0 port	DESTINATION	
	UMA	Dis
0	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
1	USB 2.0(right side)	USB 2.0(right side)
2	USB 2.0(right side)	USB 2.0(right side)
3	WLAN/BT	WLAN/BT
4	Camera	Camera
5	Touch screen(Options)	Touch screen(Options)
6	X	X
7	X	X

### <PCI-E,SATA,USB3.0>

Lane#	PCI-E	SATA	USB3.0	DESTINATION	
				UMA	Dis
1			1	USB3.0	USB3.0
2			2	X	X
3	1		3	X	X
4	2		4	Card reader(PCI-E)	Card reader(PCI-E)
5	3			10/100/1000 LAN	10/100/1000 LAN
6	4				
7	5				GPU(DIS only)
8					GPU(DIS only)
9					GPU(DIS only)
10					GPU(DIS only)
11	L3	3		WLAN	WLAN
12	L2	2		X	X
13	L1	1		ODD	ODD
14	L0	0		2.5"HDD	2.5"HDD

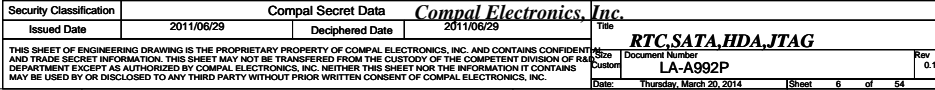


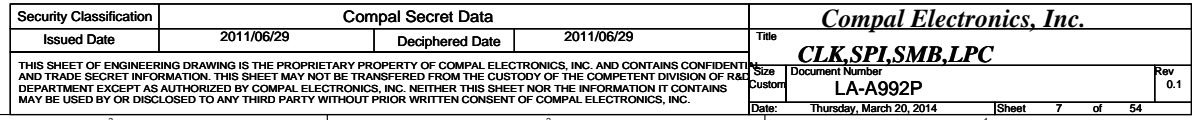
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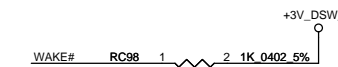
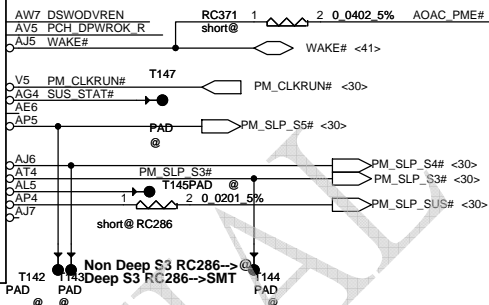
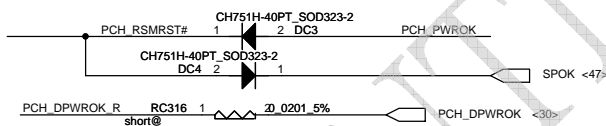
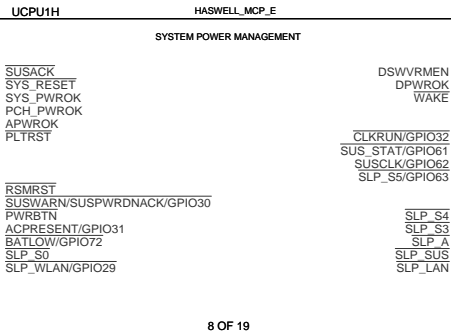
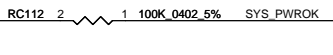
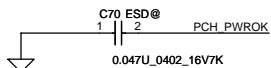
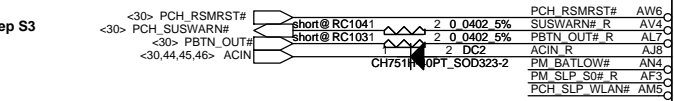
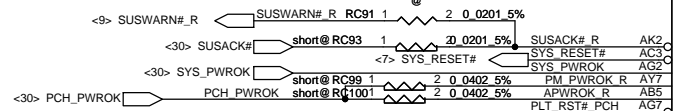
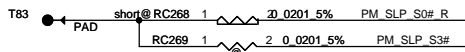
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	DDRIII	
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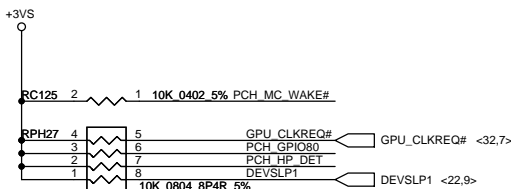
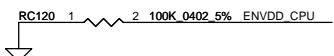
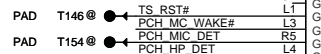
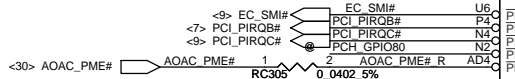
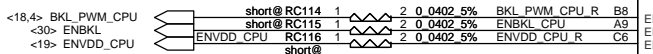
Non Deep S3 RC91-->SMT  
Deep S3 RC93-->SMT

Deep S3



Deep S3:DSW power choose on page12

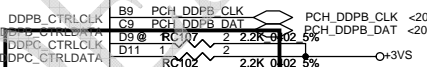
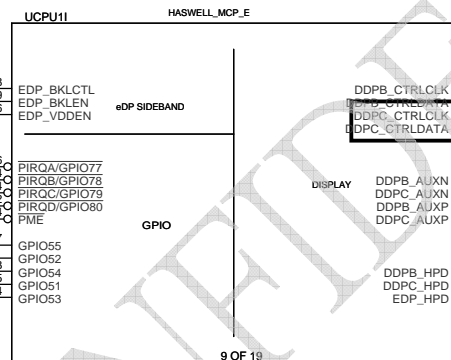
PANEL\_BKEN\_CPU PD 100K on Page20



<PV>PRH18 change to RPH27.



PD on KBC page

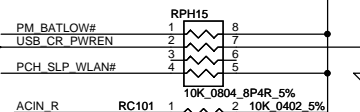


<S>Displayport Port C Enable pin RC102 pull high +3VS

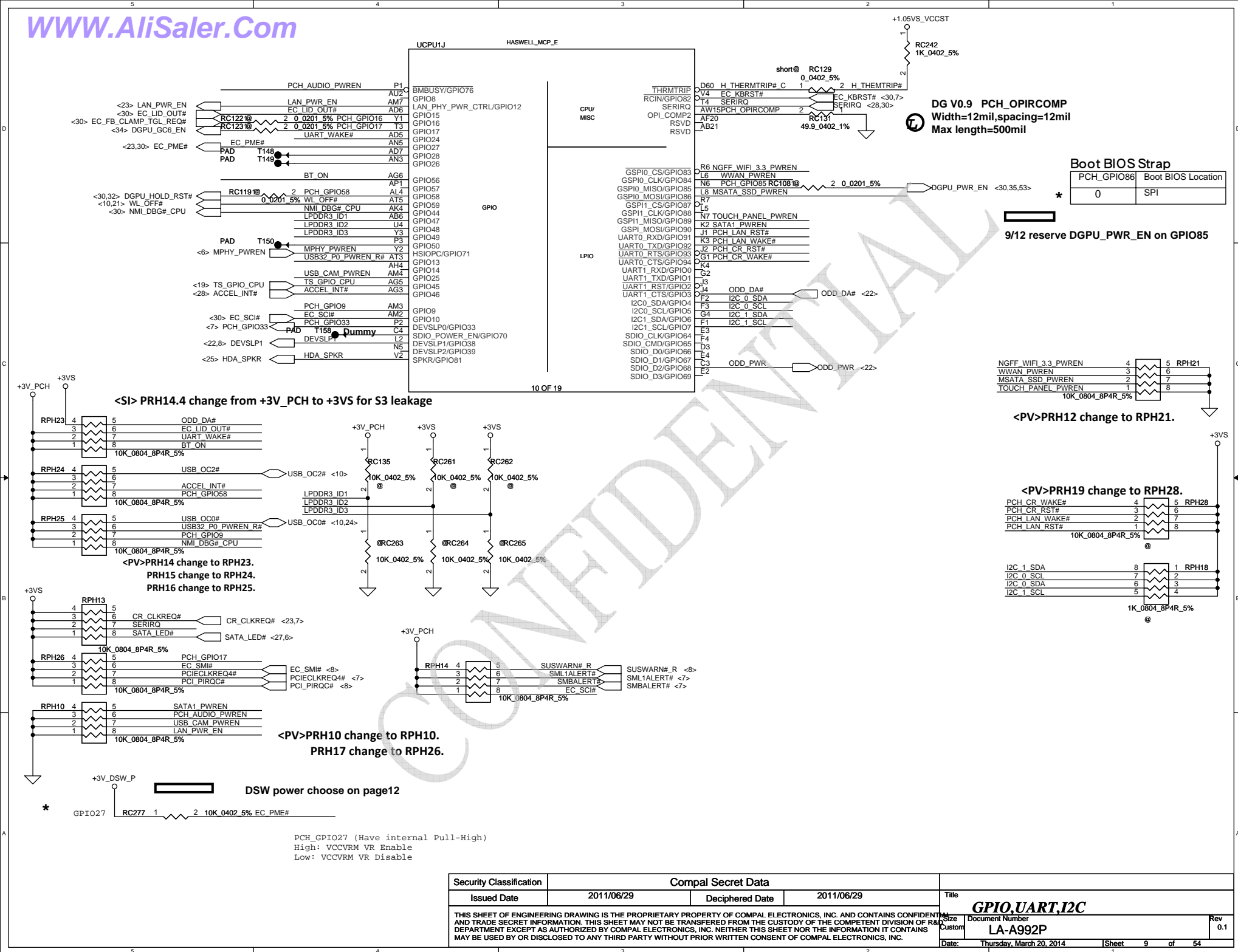
<HDMI>

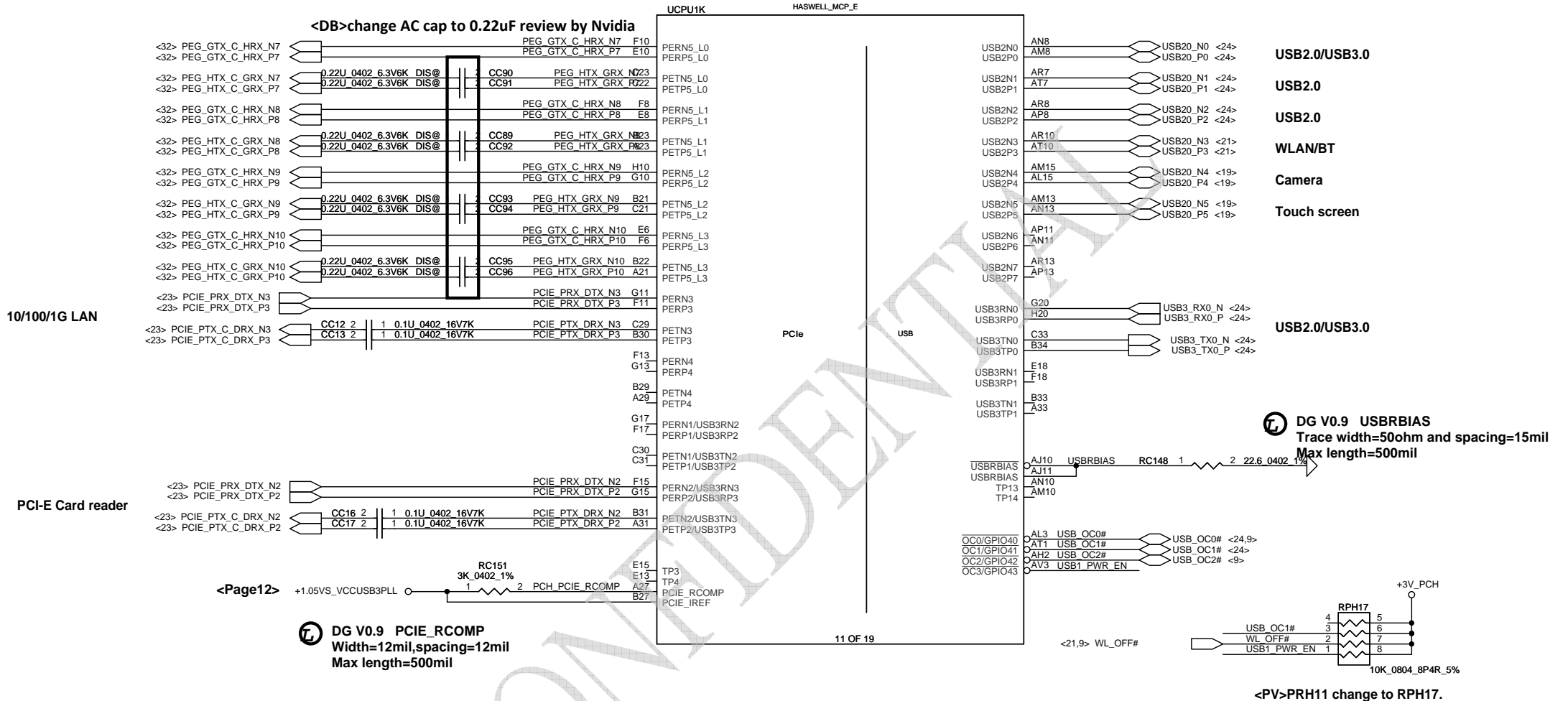
<DP TO CRT HPD>

<HDMI>  
<DP TO CRT HPD>  
<eDP HPD>



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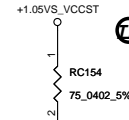


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	<b>PCIE,USB</b>	
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+VCC\_CORE@10000mA

+VCC\_CORE

## SVID ALERT



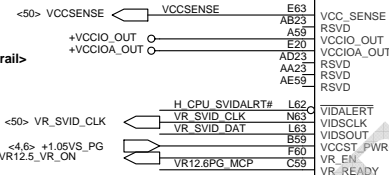
DG V0.5 H\_CPU\_SVIDALRT#  
RC154 close to CPU<300mil  
Max length=1000~2000mil

## VCC\_SENSE

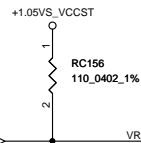
**<PWR VR12.6>**

<VR IV and CPU>  
<EDP\_COMP power

PH on power page

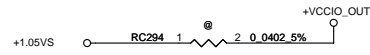


## SVID DATA



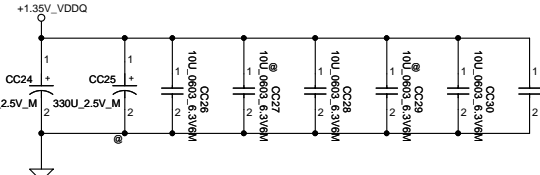
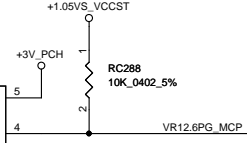
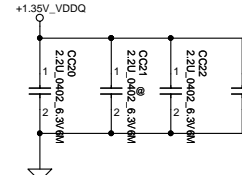
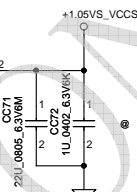
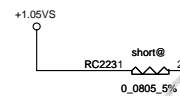
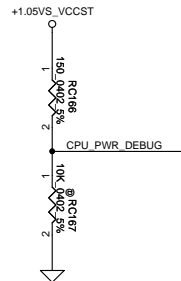
<PWR VR12.6>

**<CPU>**



+VCC\_CORE 600mA

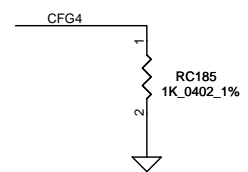
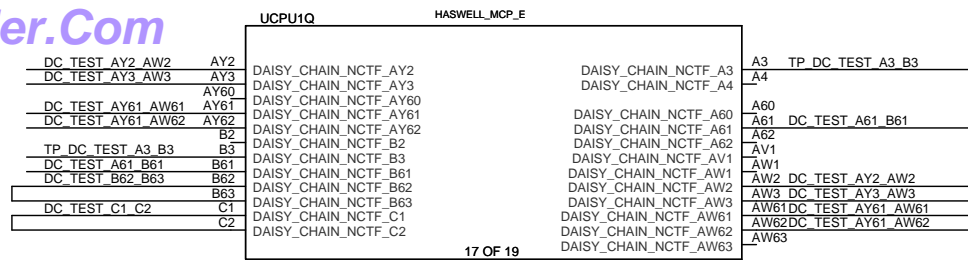
**Ⓛ** DG V0.5 VIDSOUT  
RC156 close to CPU<500mil  
Max length=1000~2000mil



Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	<b>Power</b>	
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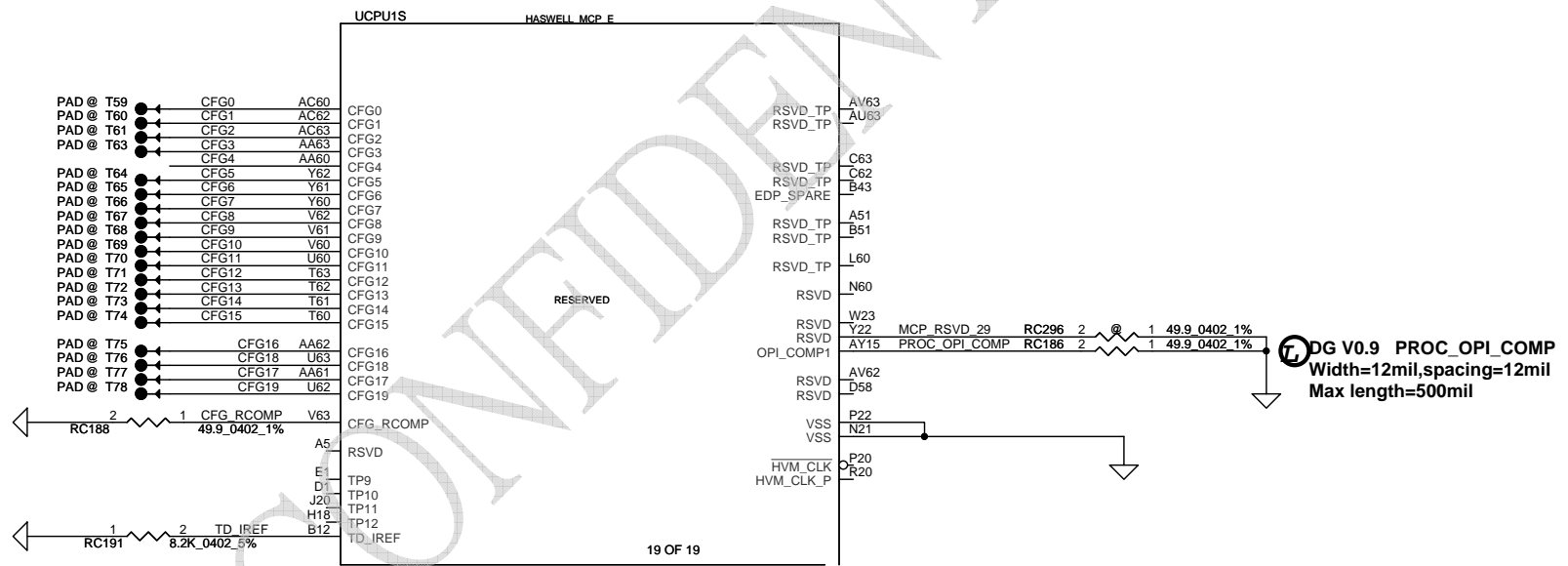
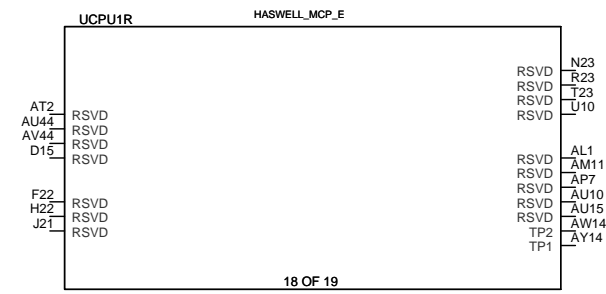


**Display Port Presence Strap**

**CFG4**

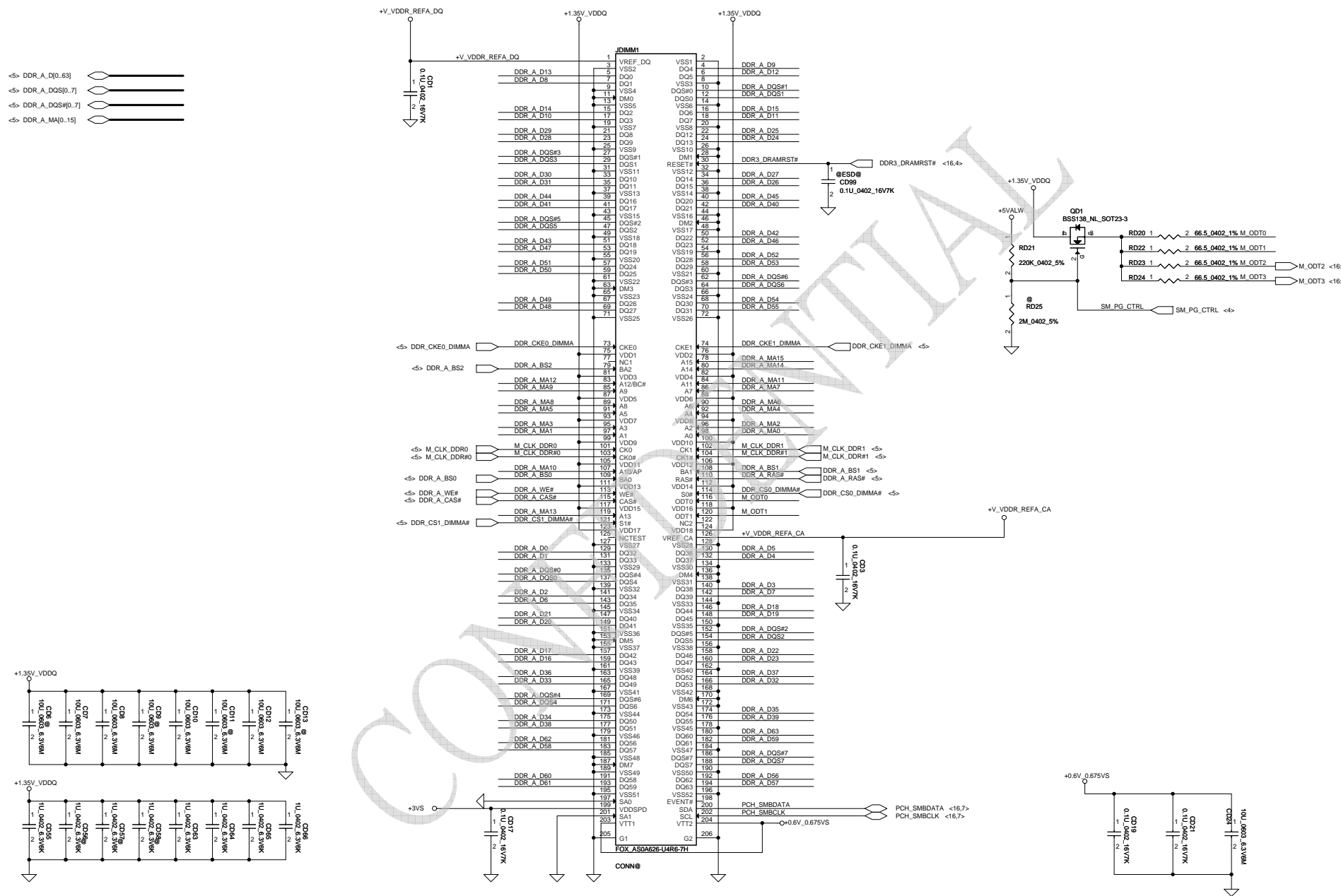
**1 : Disabled; No Physical Display Port attached to Embedded Display Port**

**\* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port**

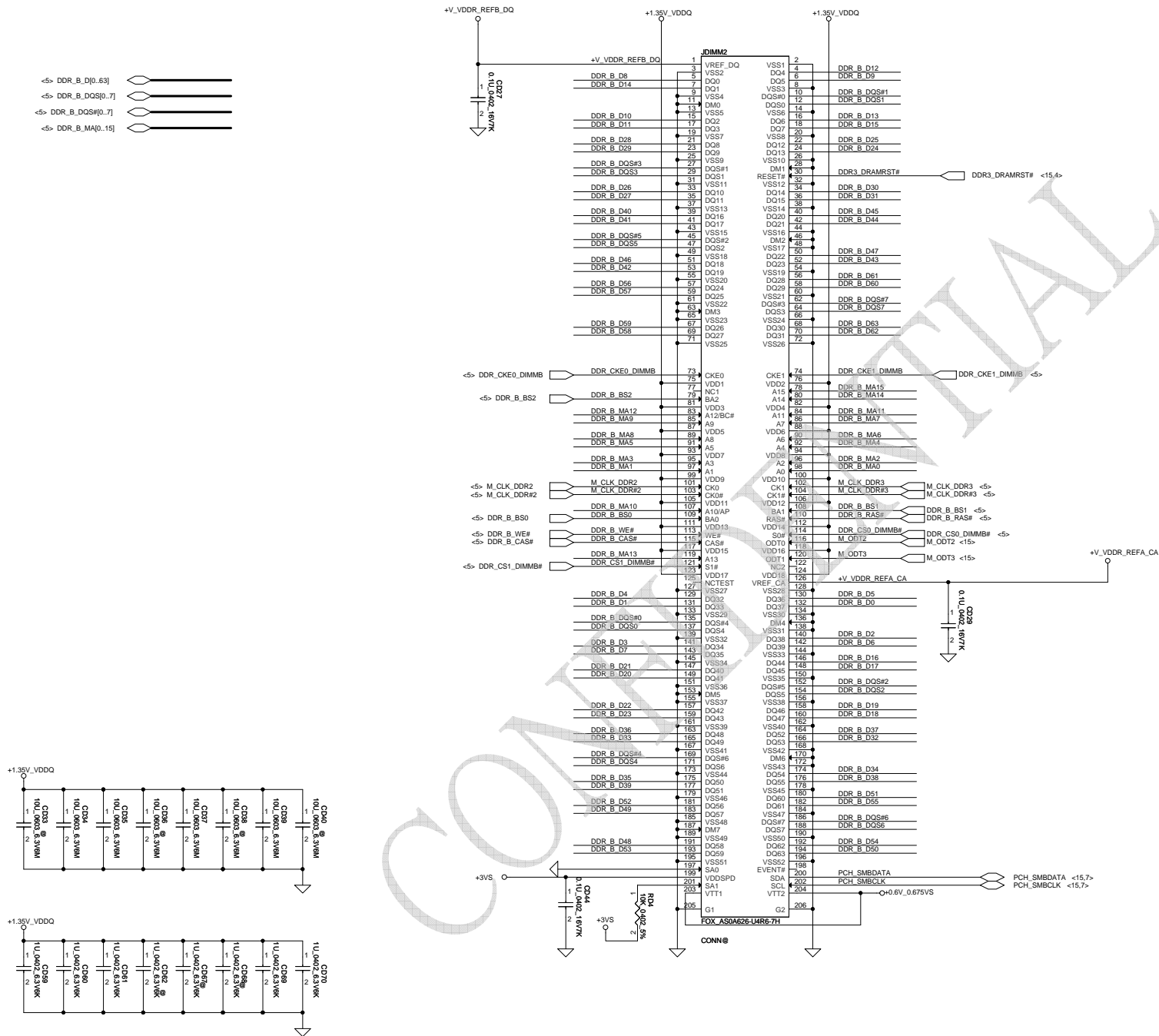


**0.9 V0.9 PROC\_OPI\_COMP**  
Width=12mil,spacing=12mil  
Max length=500mil

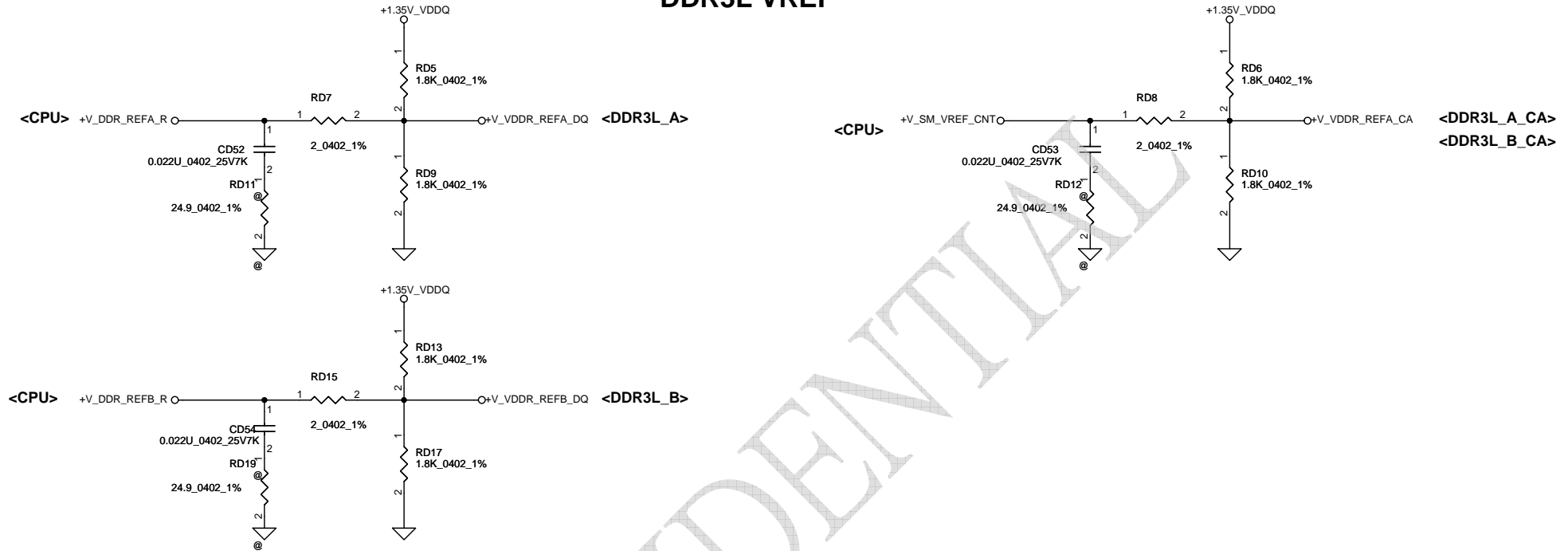
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	RSVD/CFG
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				DDR3L DIMM0	
				Size	Document Number
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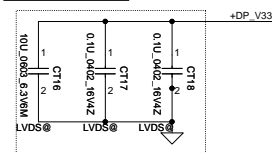
## DDR3L VREF



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JPHW7 need to short

Layout note  
Close to Pin3

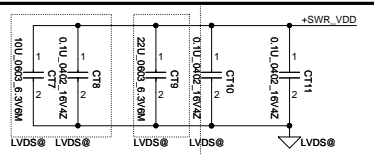


Layout note

Close to LT5

Close to Pin18

Close to Pin13



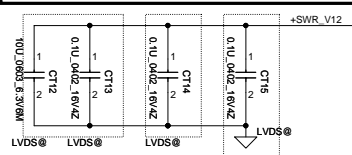
Layout note

Close to

Close to Pin11

Pin27

Close to Pin7

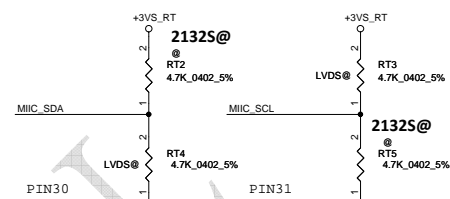


✖ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.

EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.

EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

✖Default mode



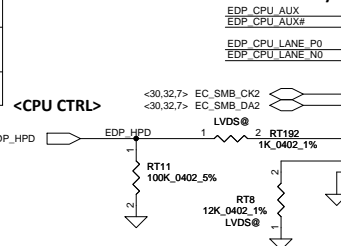
## SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

✖ If use 2132R, please select LDO mode as default.

<SI> LT7 change to 0 ohm short pad

use LDO mode translator only

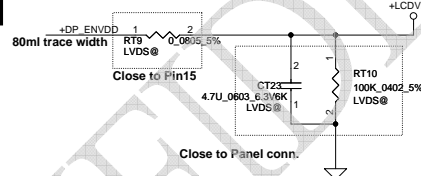


<CPU CTRL>

<CPU>

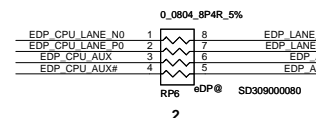
<E> EDP_CPU_AUX_C	CC102	1	2	.1U_0402_16V7K	EDP_CPU_AUX
<E> EDP_CPU_AUX#_C	CC101	1	2	.1U_0402_16V7K	EDP_CPU_AUX#
<E> EDP_CPU_LANE_P0_C	CC98	1	2	.1U_0402_16V7K	EDP_CPU_LANE_P0
<E> EDP_CPU_LANE_N0_C	CC97	1	2	.1U_0402_16V7K	EDP_CPU_LANE_N0

Layout note  
Close to Pin8

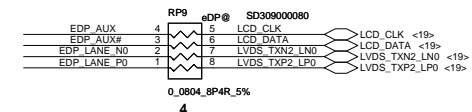


10/9 colay eDP use close Connector

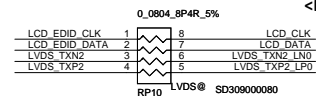
<CPU by PASS eDP>



<eDP to connector>



<LVDS to connector>

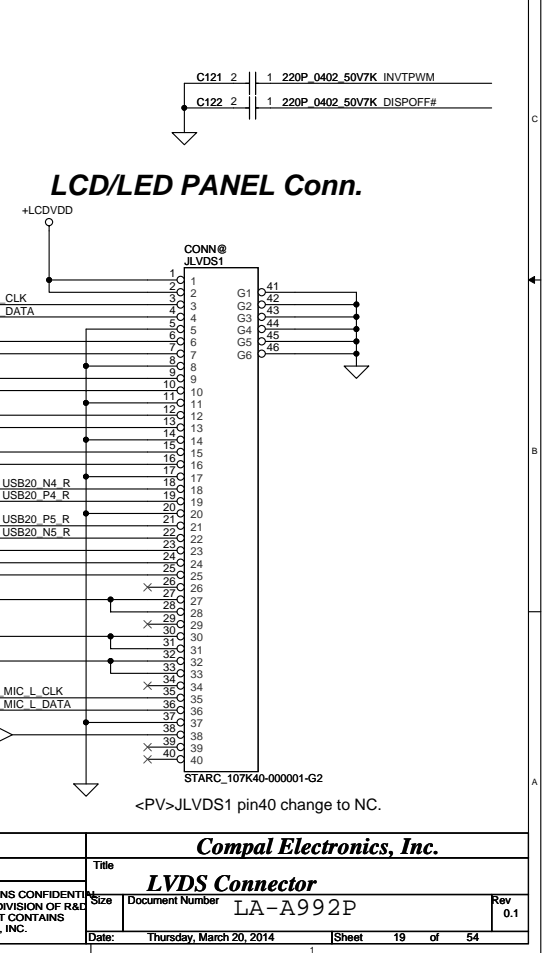
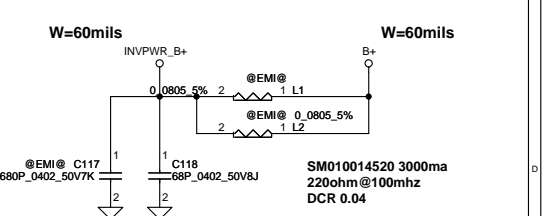


<PV>Change PR37 pin define , Add PR38.

PR37 change to RP9.

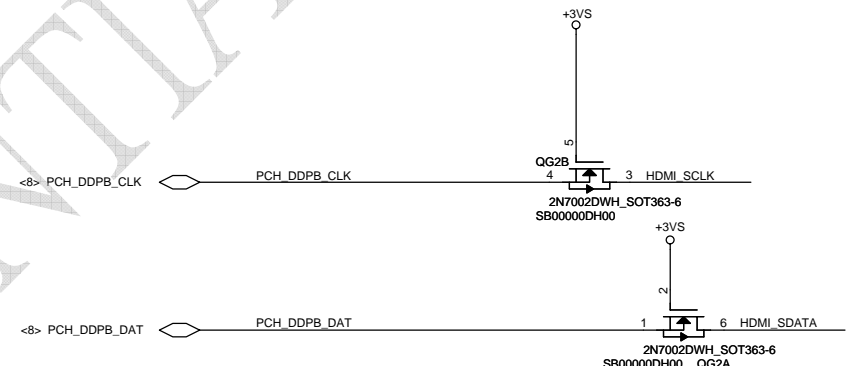
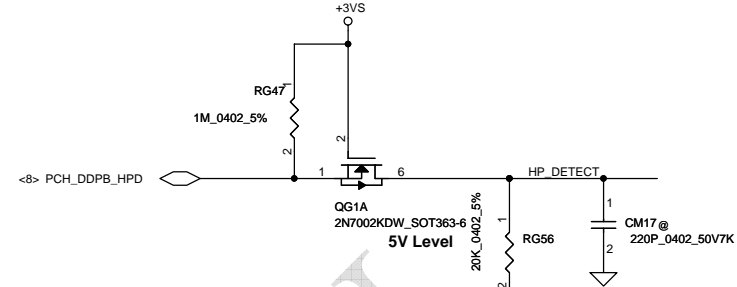
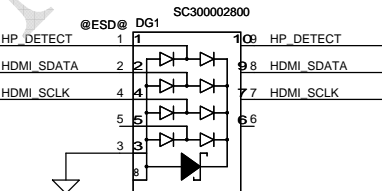
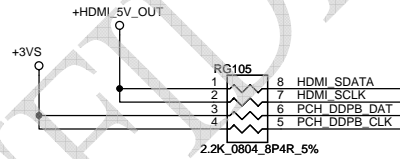
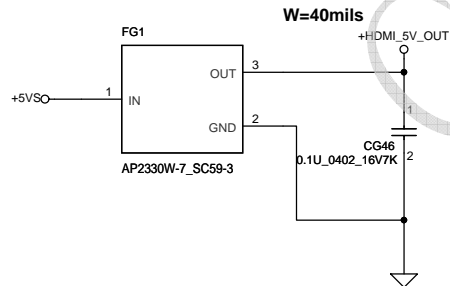
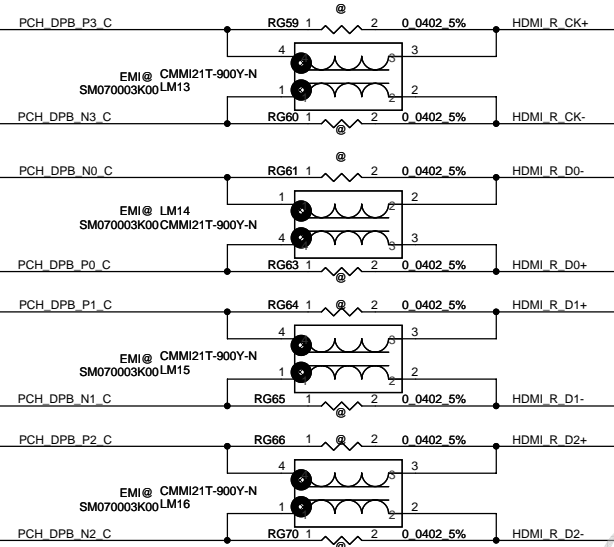
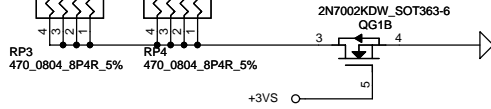
PR38 change to RP10.

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2015/3/1		Title
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LA-A992P		1.1
Date: Thursday, March 20, 2014		Sheet 18 of 54

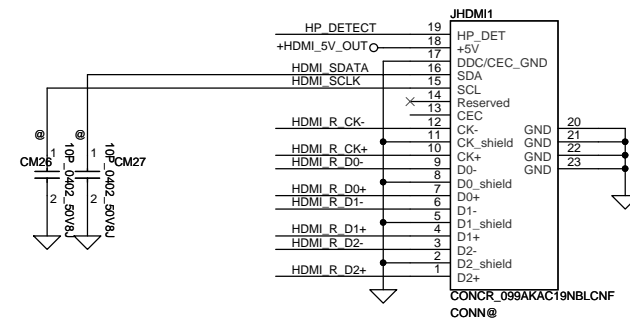


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					LA-A992P	0.1
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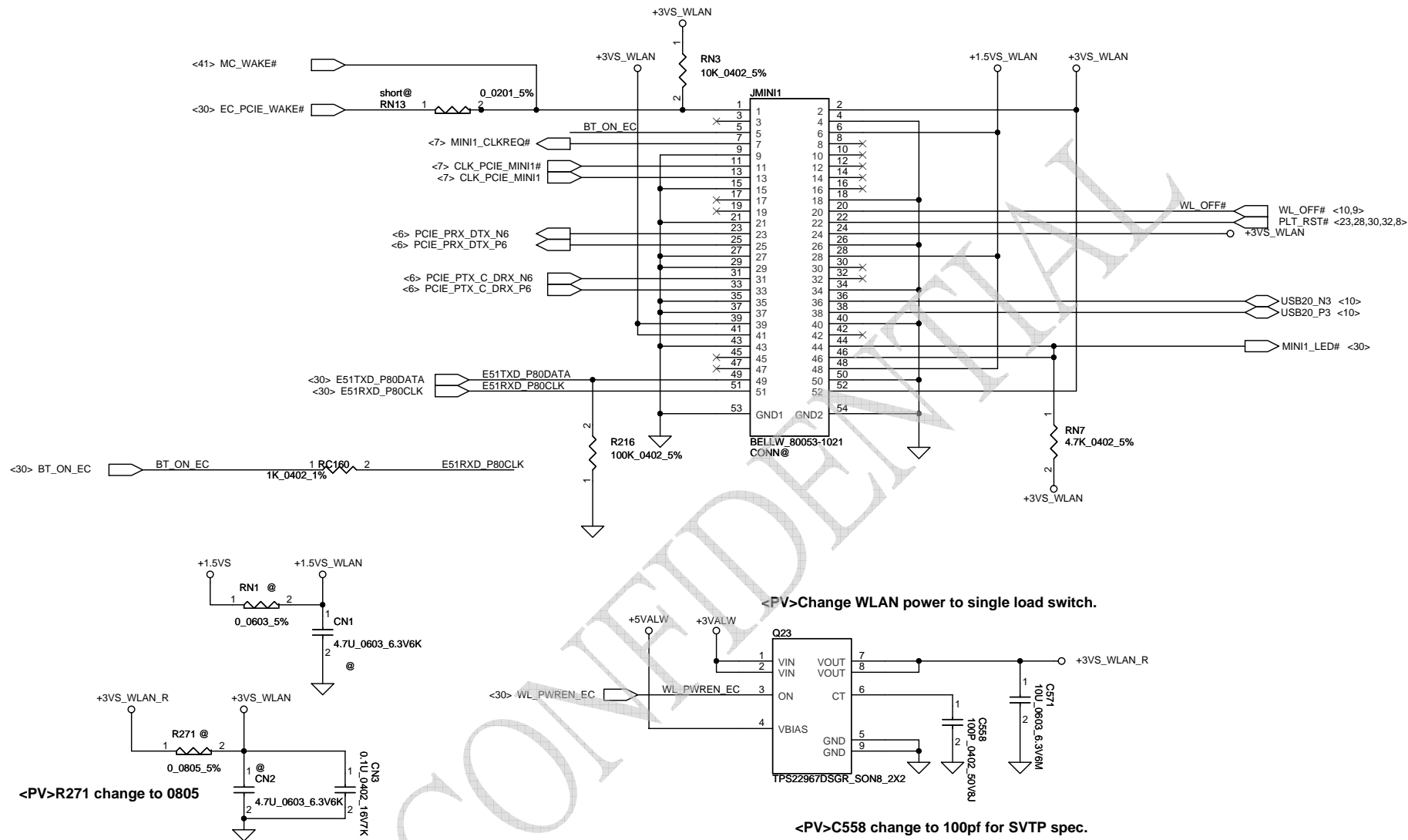
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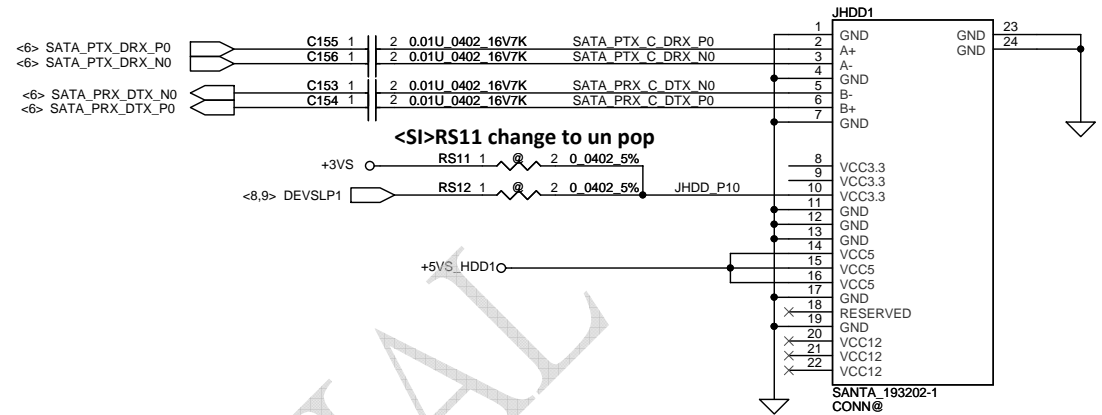
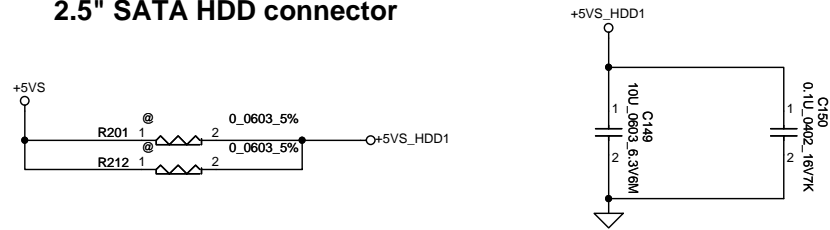
HDMI Conn.



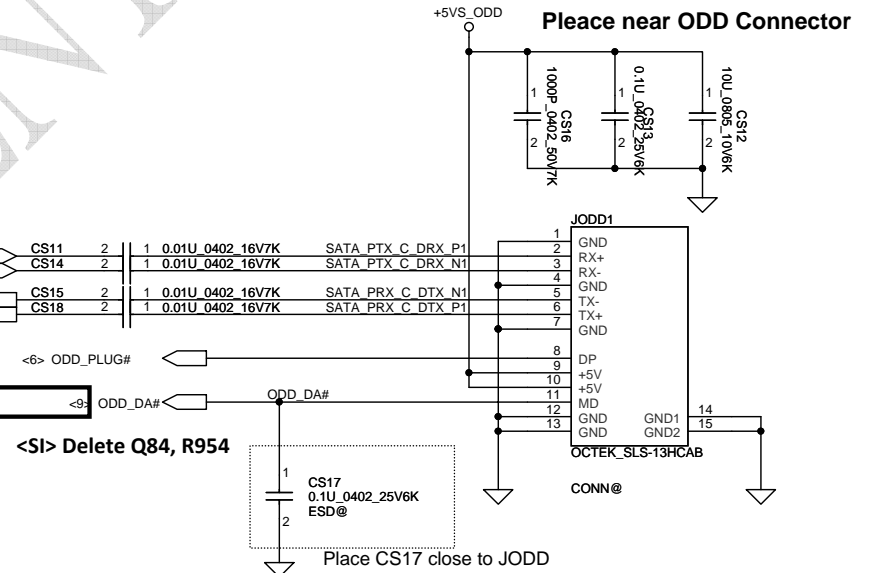
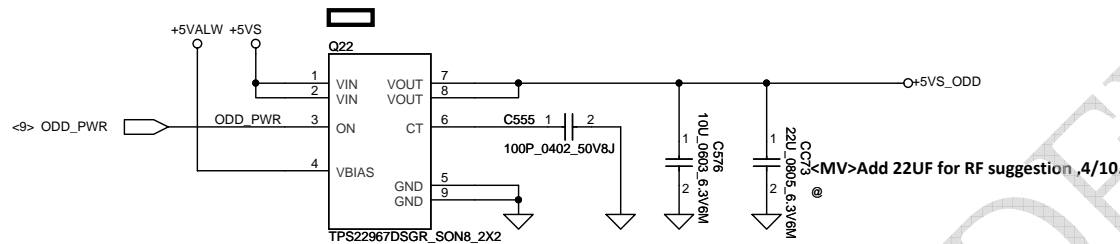
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	HDMI Conn/Level shift
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				Date	Thursday, March 20, 2014
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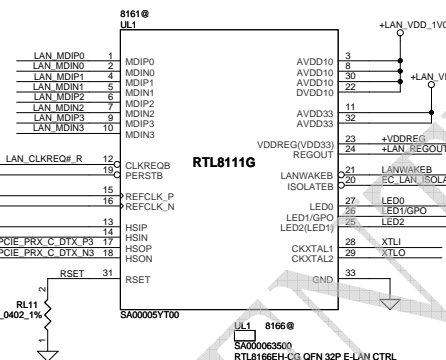
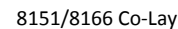
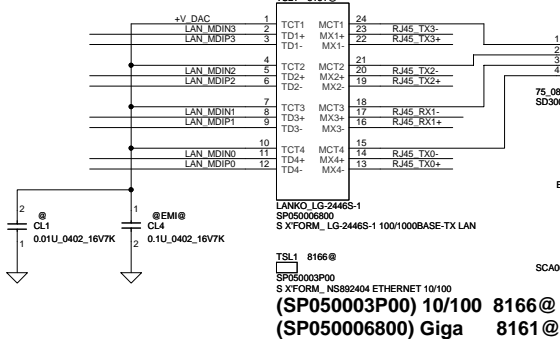
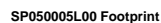
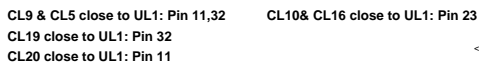
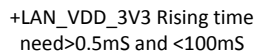
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	WLAN
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				Date:	Thursday, March 20, 2014
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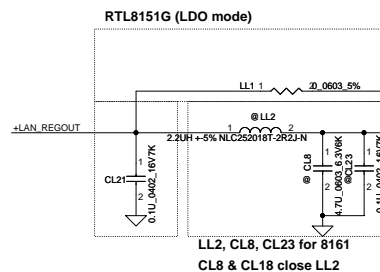
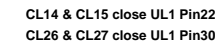
Change to dual load switch for ODD and WLAN  
<PV>Q22 change to single load switch.



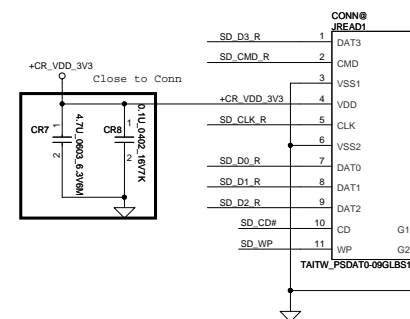
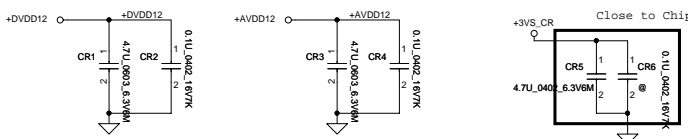
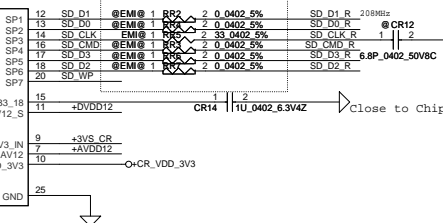
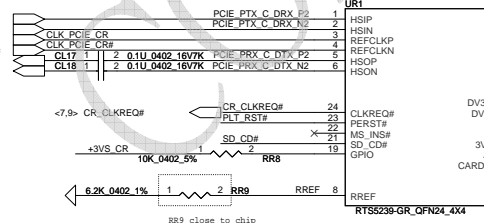
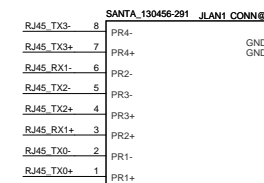
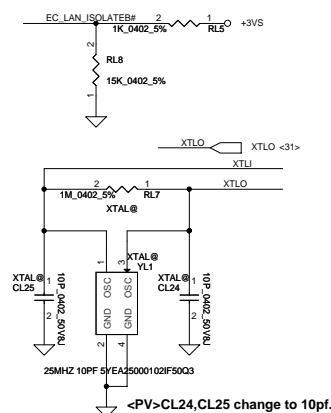
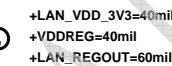
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				Date:	Thursday, March 20, 2014
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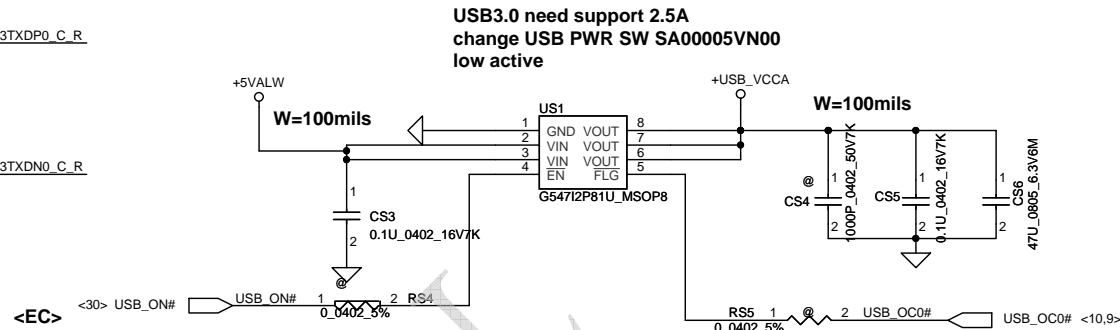
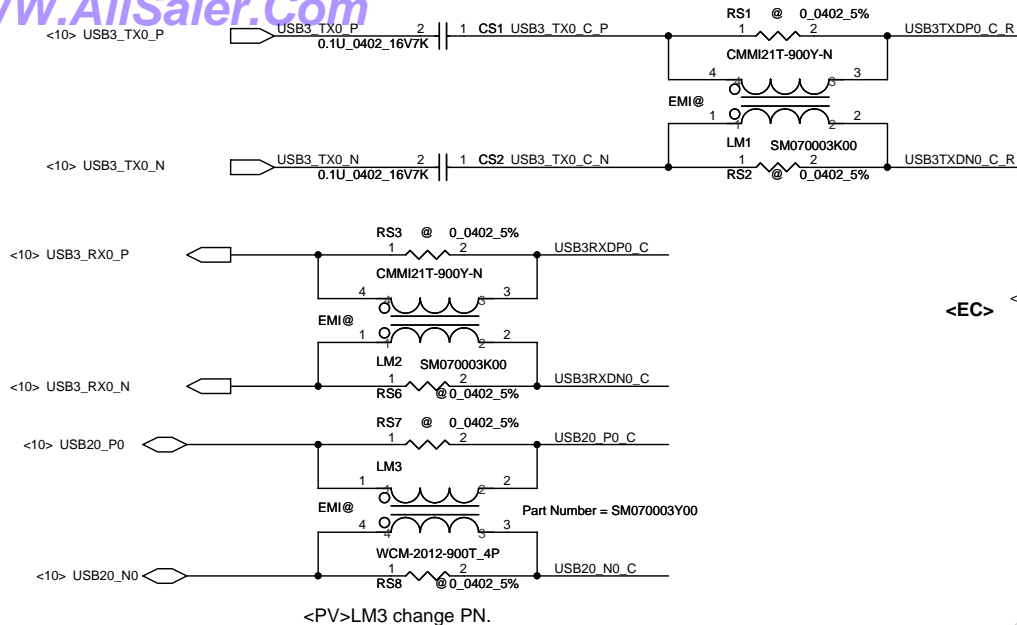
(SA000063500) 10/100 8166@  
(SA00005YT00) Giga 8151@



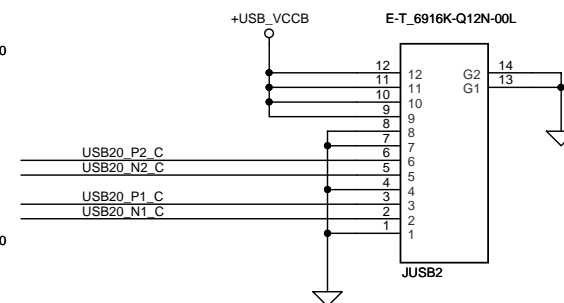
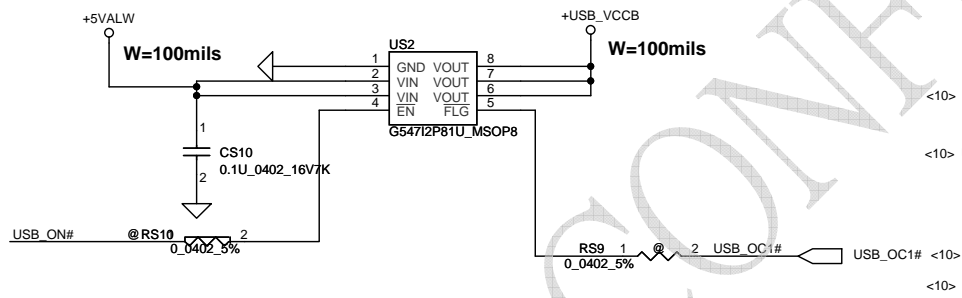
Place CL11~CL13 close UL1 Pin 3, 8 , 22



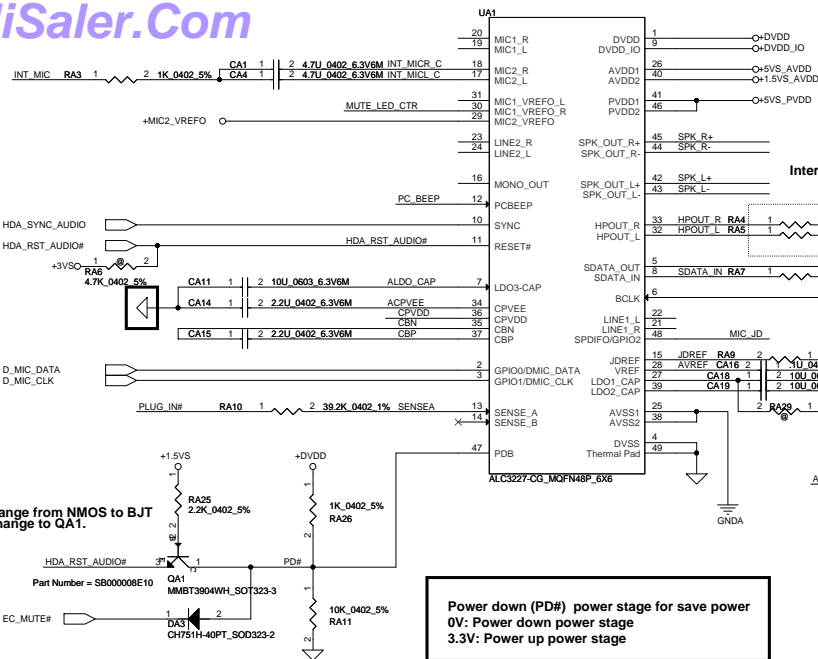
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Issued Date		2013/02/26	Deciphered Date	2015/07/08	Title	
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## USB2.0 port x 2



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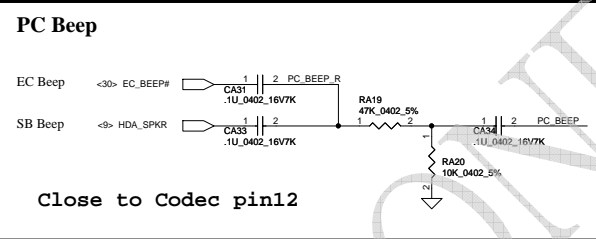
### Internal Speaker

### Headphone

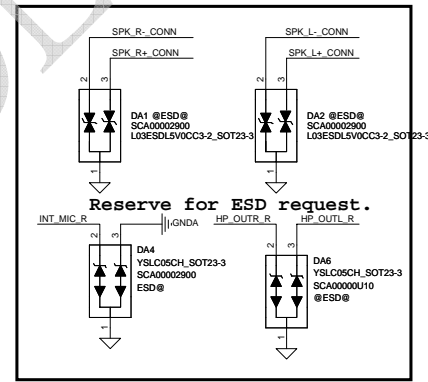
### Internal SPK

<BS> replace RA13/RA14/RA15/RA16 close to U1  
<PV> RA13-RA16 change to SM010008A00, 30-ohm.

### wide 40 MIL Delete ESD Diode

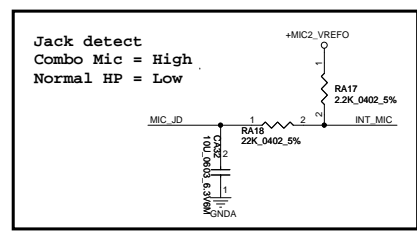


Close to Codec pin12

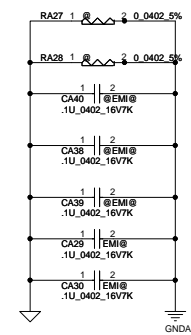


### COMBO AUDIO JACK

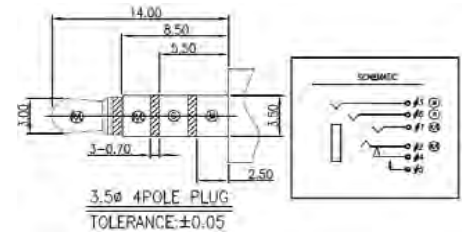
HPR, HPL, 15mil Keep 30mil



Jack detect  
Combo Mic = High  
Normal HP = Low

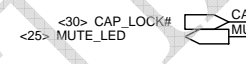
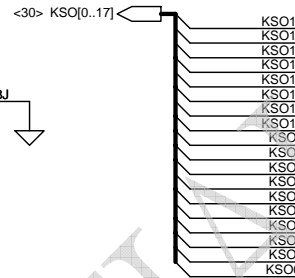
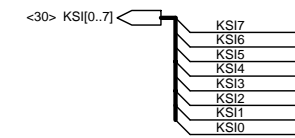
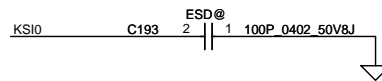
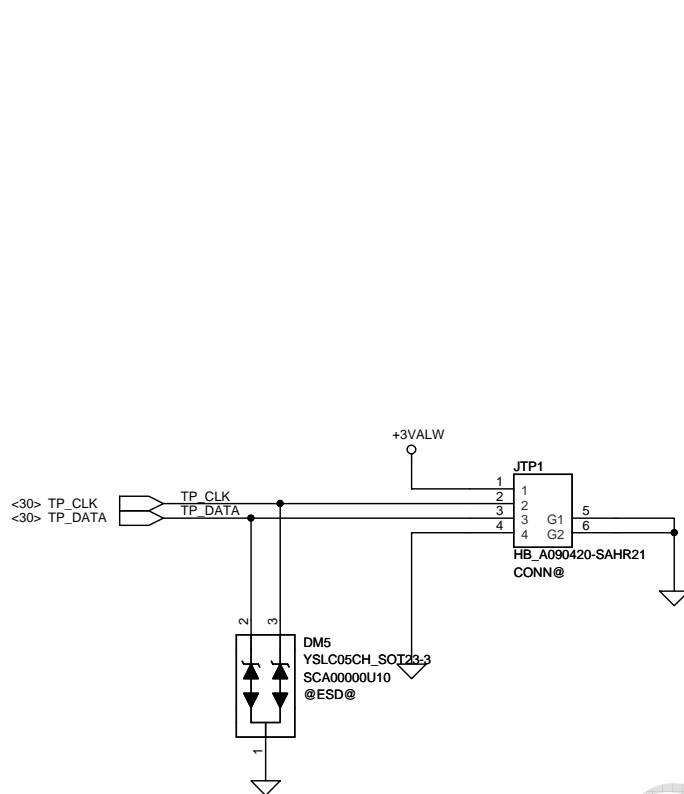


Delete ESD Diode

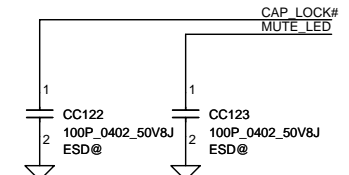
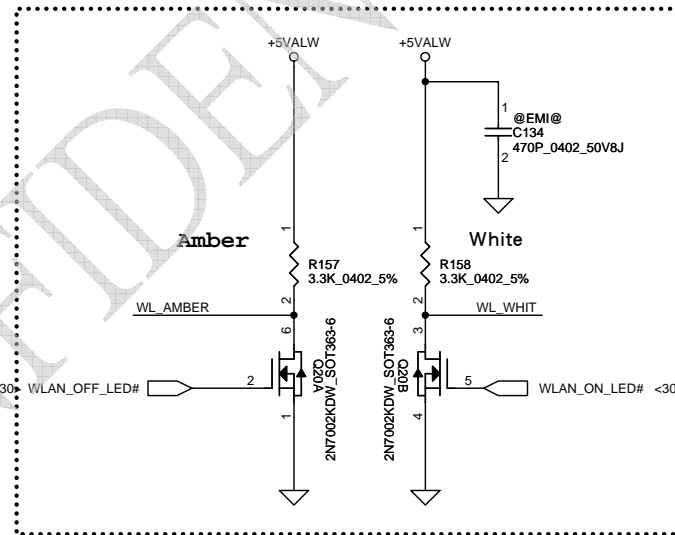
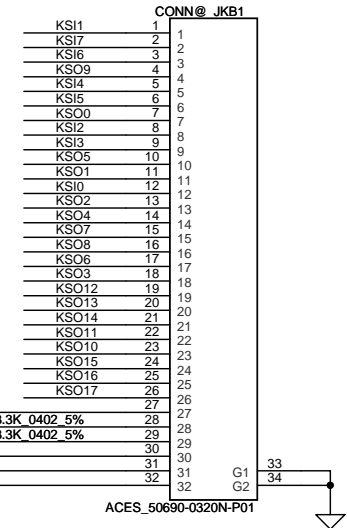


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## Touch pad conn

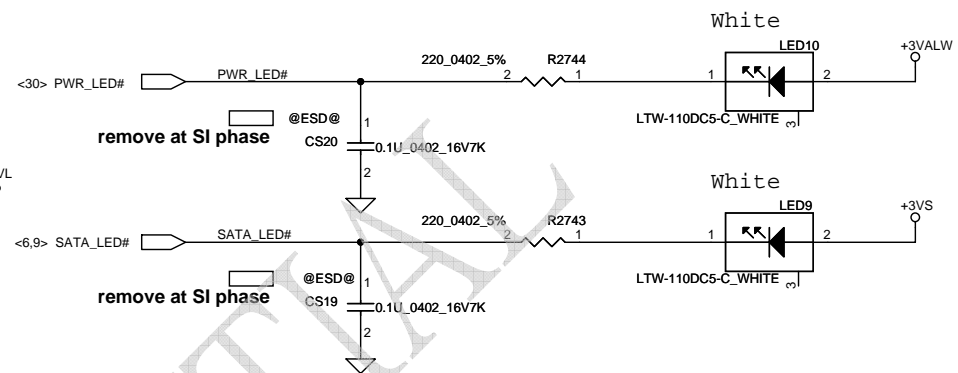
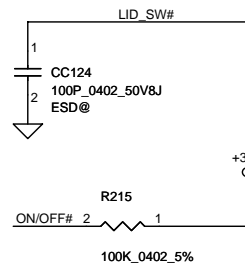
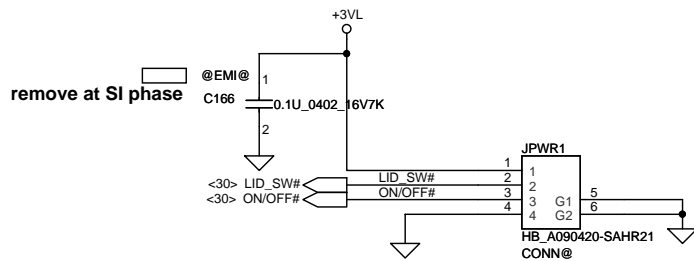


## Keyboard conn

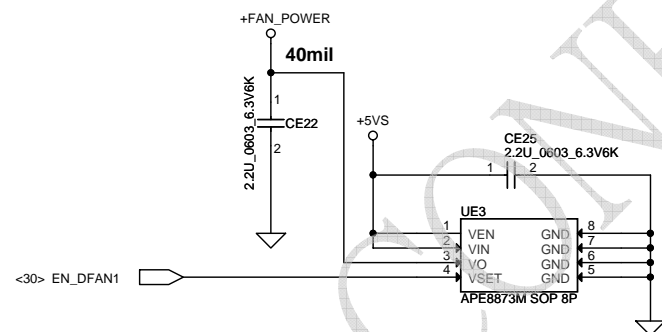


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								Document Number		Rev	
								LA-A992P		0.1	
								Date:		Thursday, March 20, 2014	
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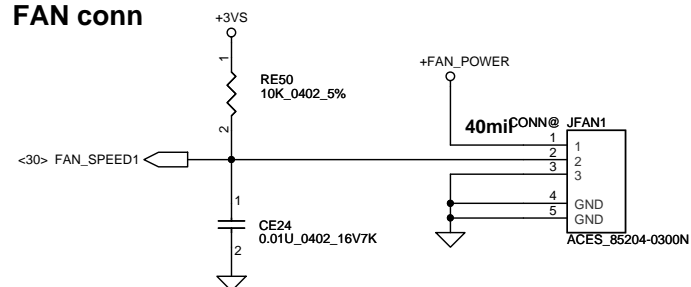
# Power Button Connector



<SI> Del New Lid SW conn

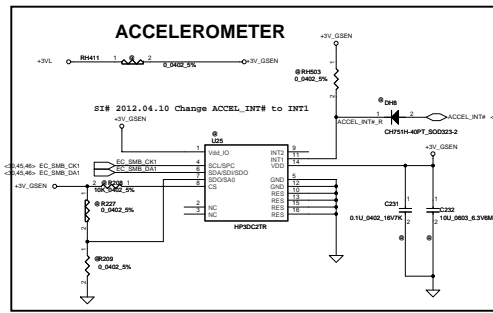



## FAN conn

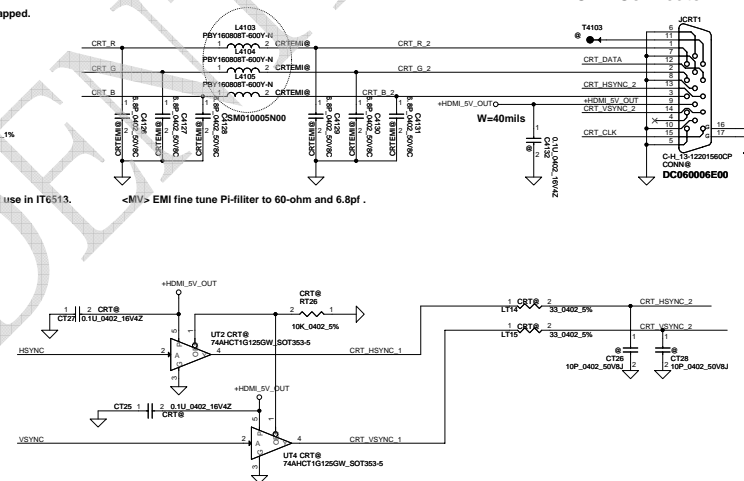
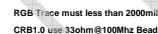
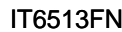
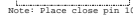
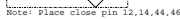


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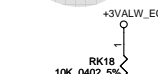
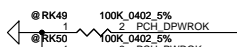
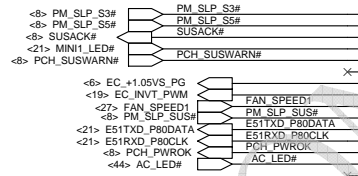
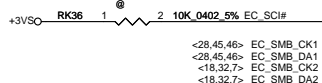
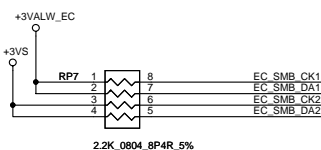
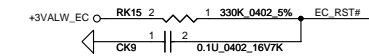
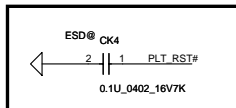


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Issued Date	2017/03/28	Deciphered Date	2017/07/08	Yes
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			Drawn	10/26/2016 20:25:11
			Printed	2017/07/08 14:54

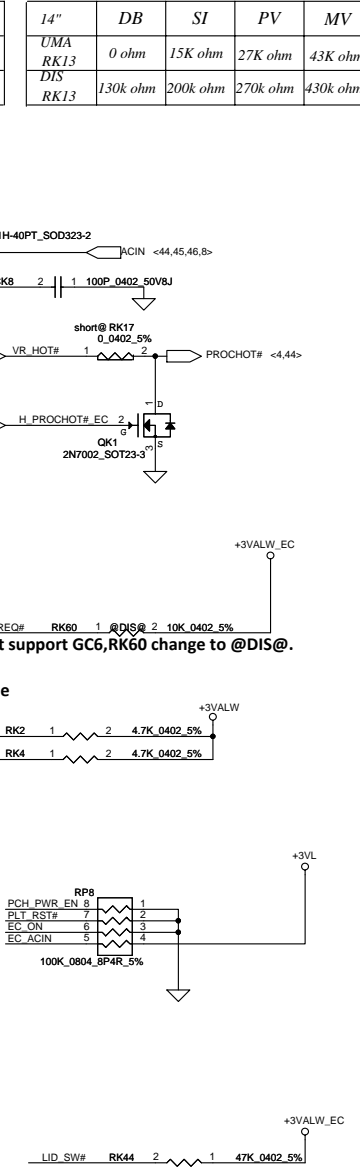
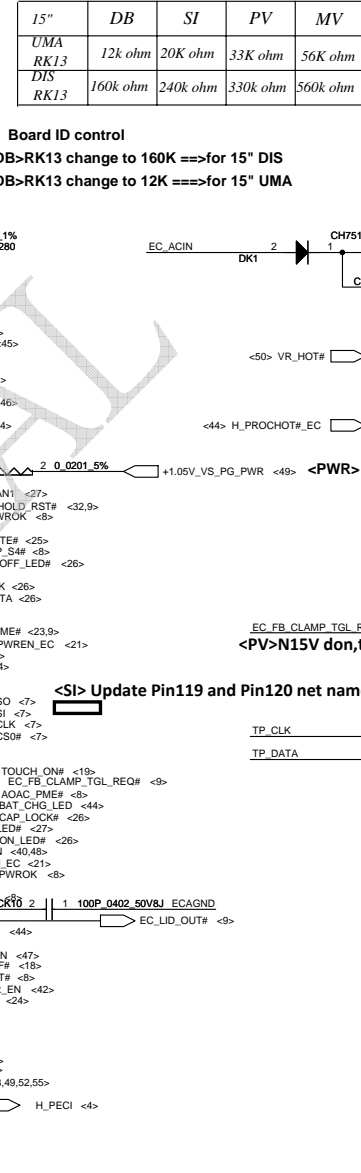
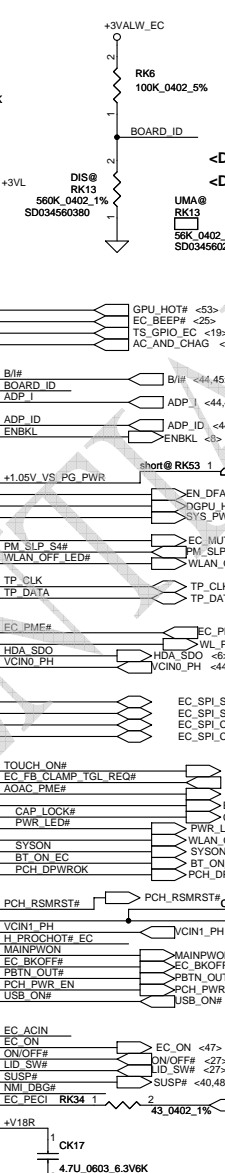
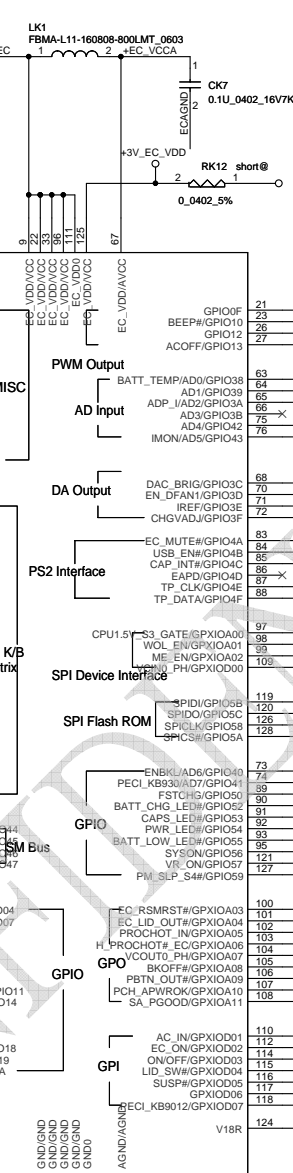


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Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	eDP to CRT
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PV# 2013.01.29 Add CK4 for ESD protection



KB90120F-A3 LQFP128, 14X14  
Part Number = SA000040B30



Board ID control  
<DB>RK13 change to 160K ==>for 15" DIS  
<DB>RK13 change to 12K ==>for 15" UMA

<S1> Update Pin119 and Pin120 net name

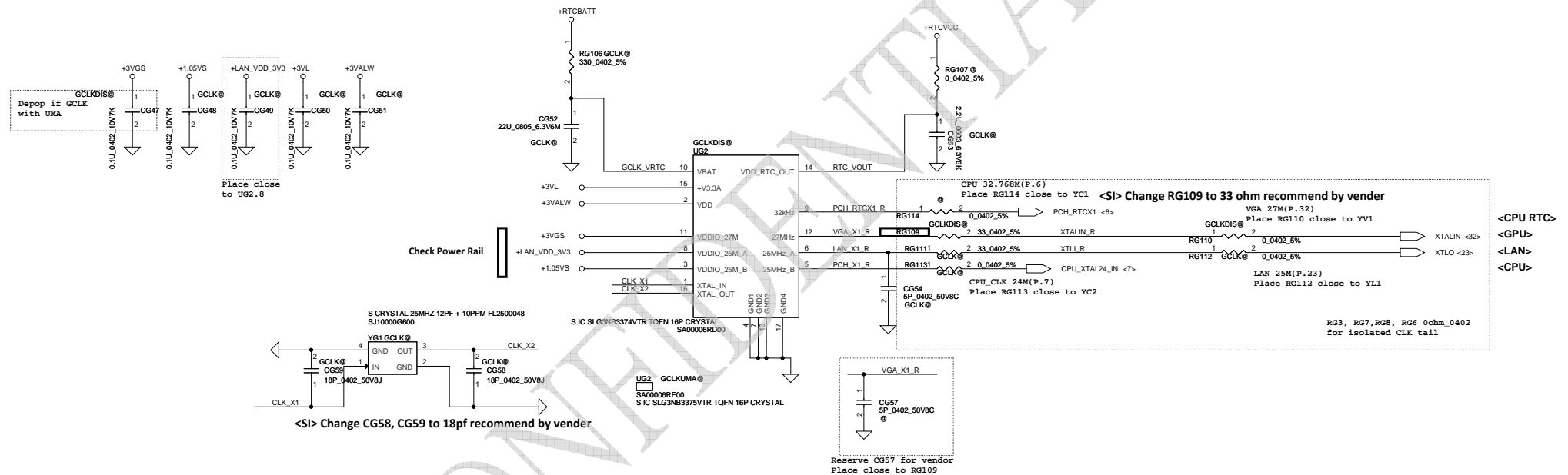
<PV>N15V don't support GC6,RK60 change to @DIS@.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	EC ENE-KB9012
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				Custom	LA-A992P
				Date	Thursday, March 20, 2014
				Sheet	30 of 54

BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3375V	SA00006RE00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3374V	SA00006RD00	1	1	1	1	X	GCLKDIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.



#9/2 , Add RV191 between.  
GPU\_PWR\_LEVEL# and GPU\_THERMAL\_DET#

GPU_PWR_LEVEL#	RV62	1	DIS@	2	100K_0402_5%
GPU_GPIO6	RV43	1	DIS@	2	10K_0402_5%
NVDD_PSI	RV44	1	DIS@	2	10K_0402_5%
GPU_GPIO8	RV46	1	DIS@	2	10K_0402_5%
GPU_GPIO9	RV48	1	DIS@	2	10K_0402_5%

&lt;CPU&gt;

<10>	PEG_HTX_C_GRX_P7	PEG_HTX_C_GRX_P7	AG6
<10>	PEG_HTX_C_GRX_N7	PEG_HTX_C_GRX_N7	AG7
<10>	PEG_HTX_C_GRX_P8	PEG_HTX_C_GRX_P8	AF7
<10>	PEG_HTX_C_GRX_N8	PEG_HTX_C_GRX_N8	AE7
<10>	PEG_HTX_C_GRX_P9	PEG_HTX_C_GRX_P9	AE8
<10>	PEG_HTX_C_GRX_N9	PEG_HTX_C_GRX_N9	AF9
<10>	PEG_HTX_C_GRX_P10	PEG_HTX_C_GRX_P10	AG9
<10>	PEG_HTX_C_GRX_N10	PEG_HTX_C_GRX_N10	AG10

PEX_RX0	AG6
PEX_RX0_N	AG7
PEX_RX1	AF7
PEX_RX1_N	AE7
PEX_RX2	AE8
PEX_RX2_N	AF9
PEX_RX3	AG9
PEX_RX3_N	AG10
PEX_RX4	AG11
PEX_RX4_N	AG12
PEX_RX5	AG13
PEX_RX5_N	AG14
PEX_RX6	AF13
PEX_RX6_N	AF14
PEX_RX7	AE13
PEX_RX7_N	AE14
NC	AF15
NC	AG15
NC	AG16
NC	AF16
NC	AE16
NC	AE18
NC	AF18
NC	AG18
NC	AG19
NC	AF19
NC	AE19
NC	AE21
NC	AF21
NC	AG21
NC	AG22

Part 1 of 5

PCI EXPRESS

GPIO	C6 GPU_GPIO0
GPIO1	B2
GPIO2	D6
GPIO3	C7
GPIO4	F9
GPIO5	A3
GPIO6	B6
GPIO7	A6 GPU_GPIO8
GPIO8	F8 GPU_GPIO9
GPIO9	C5
GPIO10	E7 NVDD_PWM_VID
GPIO11	D7 GPU_PWR_LEVEL# RV191 1 DIS@ 2 0.0402_5%
GPIO12	B4 NVDD_PSI
GPIO13	B3
GPIO14	C3
GPIO15	D5
GPIO16	D4
GPIO17	C2
GPIO18	F7
GPIO19	E6
GPIO20	C4
GPIO21	
DACA_HSYNC	AE3
DACA_VSYNC	AE4
DACA_RED	AG3
DACA_BLUE	AF3
DACA_GREEN	AF4
DACA_VREF	AE2
DACA_RST	AF2
GPU_JTAG_TCK	AE5
GPU_JTAG_TDI	AE6
GPU_JTAG_TDO	AF6
GPU_JTAG_TMS	AD6
GPU_JTAG_TRST_N	AG4
TESTMODE	AD9
I2CA_SCL	B7 I2CA_SCL RV14 1 DIS@ 2 2.2K_0402_5%
I2CA_SDA	A7 I2CA_SDA RV15 1 DIS@ 2 2.2K_0402_5%
I2CB_SCL	C9 I2CB_SCL
I2CB_SDA	C8 I2CB_SDA
I2CC_SCL	A9 I2CC_SCL
I2CC_SDA	B9 I2CC_SDA
I2CS_SCL	D9 I2CS_SCL RV21 1 DIS@ 2 2.2K_0402_5%
I2CS_SDA	D8 I2CS_SDA RV22 1 DIS@ 2 2.2K_0402_5%
XTAL_SSIN	A10 XTALSSIN RV23 1 DIS@ 2 10K_0402_5%
XTAL_OUTBUFF	C10 XTALOUT RV25 1 DIS@ 2 10K_0402_5%
XTAL_OUT	B10 XTAL_OUT
XTAL_IN	C11 XTALIN
NC	AB6
NC	D10
NC	E9

#8/19 ,N15V-GM didn't support GC6,  
unpop QV13 ,QV14.

&lt;CPU&gt;

<10>	PEG_GTX_C_HRX_P7	PEG_GTX_C_HRX_P7 CV1	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_P7	AC9
<10>	PEG_GTX_C_HRX_N7	PEG_GTX_C_HRX_N7 CV2	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_N7	AB9
<10>	PEG_GTX_C_HRX_P8	PEG_GTX_C_HRX_P8 CV3	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_P8	AB10
<10>	PEG_GTX_C_HRX_N8	PEG_GTX_C_HRX_N8 CV4	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_N8	AC10
<10>	PEG_GTX_C_HRX_P9	PEG_GTX_C_HRX_P9 CV5	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_P9	AD11
<10>	PEG_GTX_C_HRX_N9	PEG_GTX_C_HRX_N9 CV6	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_N9	AC11
<10>	PEG_GTX_C_HRX_P10	PEG_GTX_C_HRX_P10 CV7	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_P10	AD12
<10>	PEG_GTX_C_HRX_N10	PEG_GTX_C_HRX_N10 CV8	DIS@ 1	2	2.2UJ 0402 6.3V6K	PEG_GTX_HRX_N10	AB12

&lt;CPU&gt;

&lt;7&gt; CLK\_PCIE\_GPU

&lt;7&gt; CLK\_PCIE\_GPU#

Differential signal

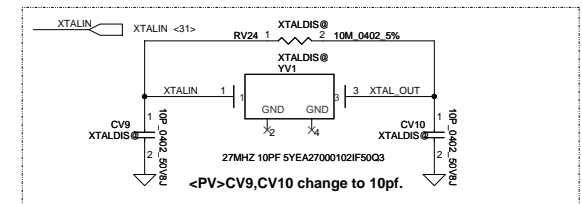
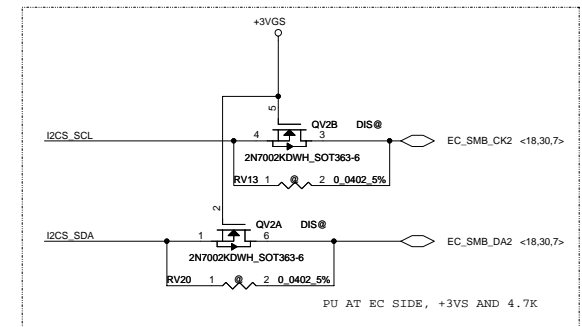
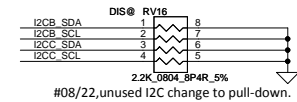
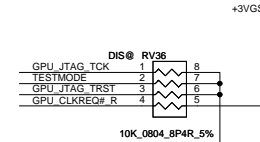
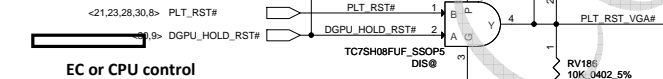
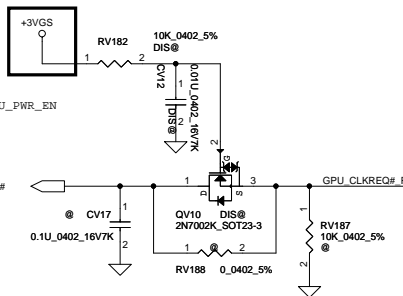
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PEX_REFCLK_N	AD8
PEX_TSTCLK_OUT	AF22
PEX_TSTCLK_OUT#	AE22
PEX_TSTCLK_OUT_N	
PEX_TERM_P	AF25
PEX_TERM_N	AC7
PLT_RST_VGA#	AC7
PEX_RST_N	AC7
GPU_CLKREQ#_R	AC6
PEX_CLKREQ#_N	

N15V-GM

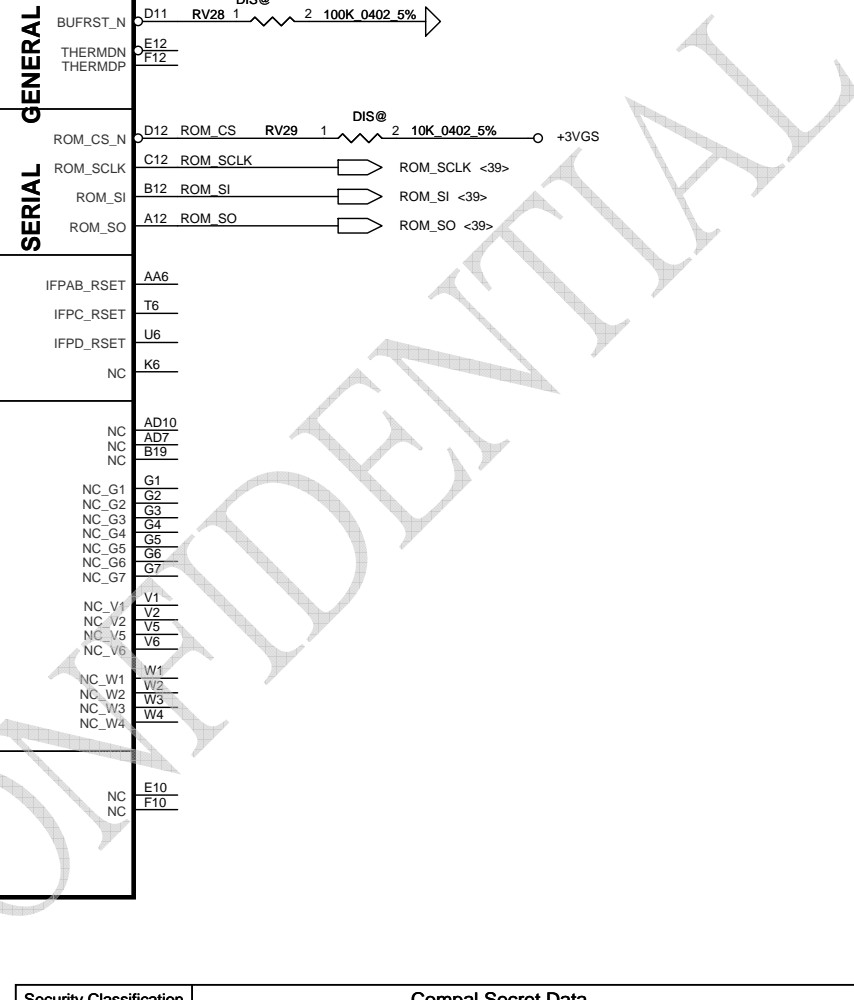
DIS@

SI 11/05 change RV182.1  
change to +3VGS from GPU\_PWR\_EN

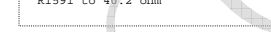
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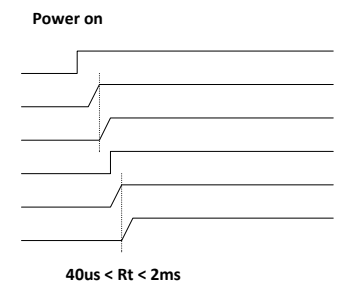
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					LA-A992P	0.1
				Date:	Thursday, March 20, 2014	Sheet 33 of 54

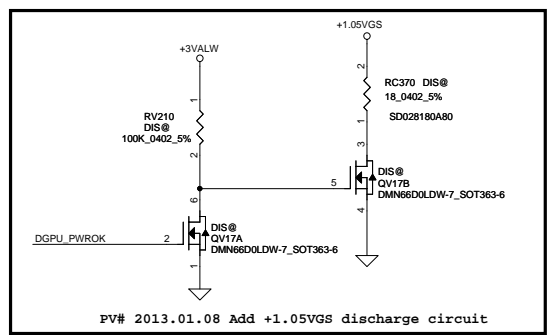
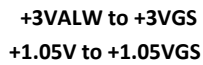


Size		Document Number	Rev
Custom	LA-A992P		0.1
Date:	Thursday, March 20, 2014	Sheet	34 of 54

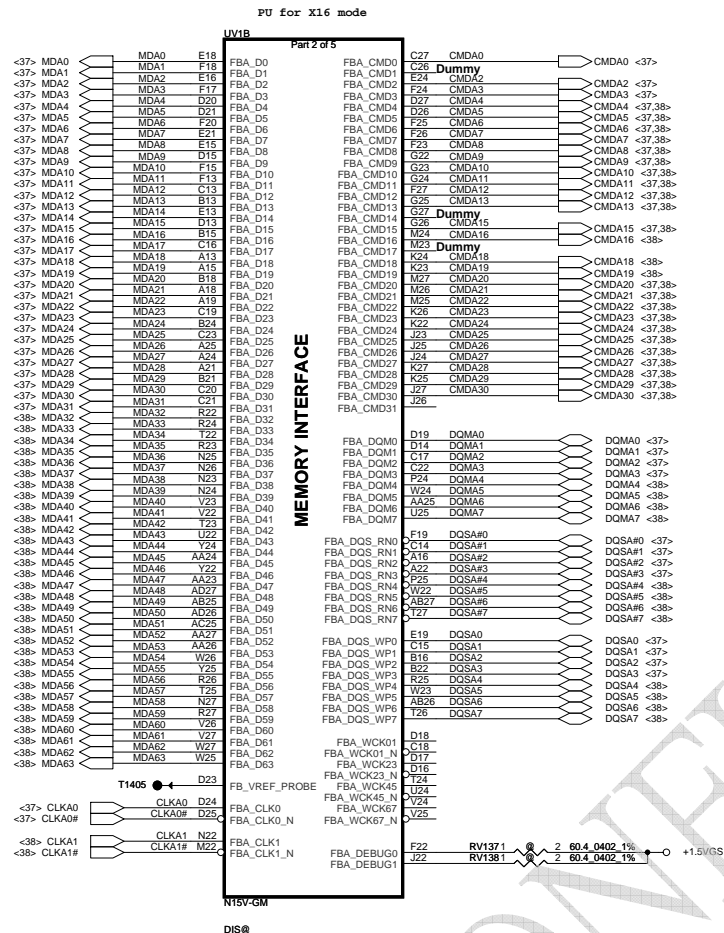


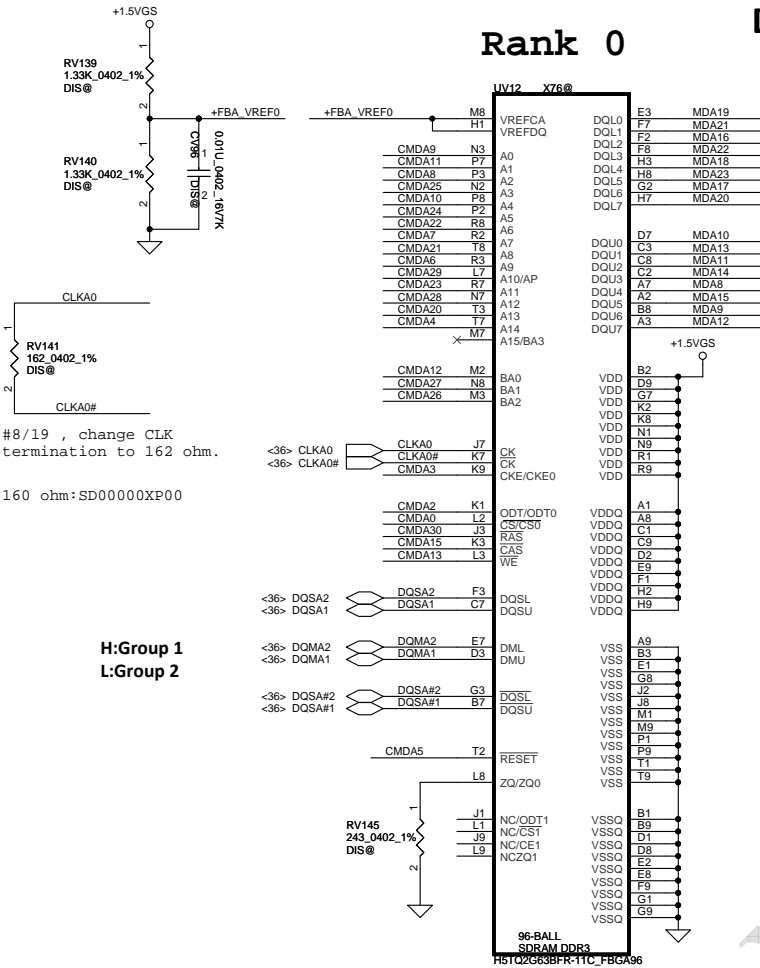
<53> DGPU\_PWROK  DGPU\_PWROK RV66 1 2  
47K 0402 5%

#08/20 Don't support GC6,Add RV66.  
Unpop QV16,RV41,RV42,CV78.



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						Size Custom
Date: Thursday, March 20, 2014						Sheet 35 of 54



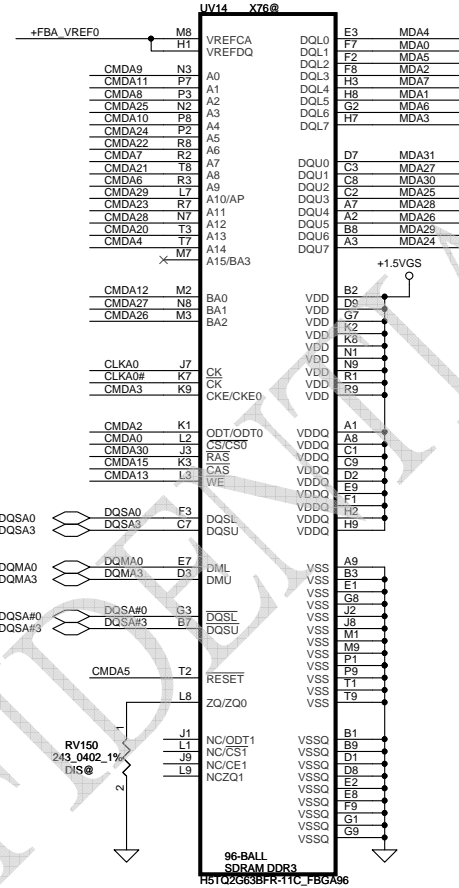


Group 2

Group 1

L:Group 0  
H:Group 3

**Rank 0**

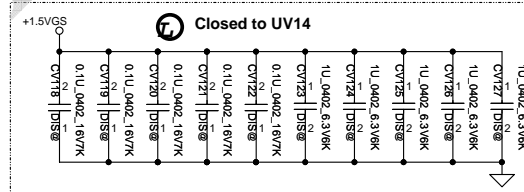
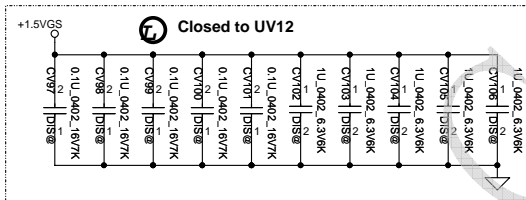


Group 0

Group 3

Mode D Command Mapping

RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

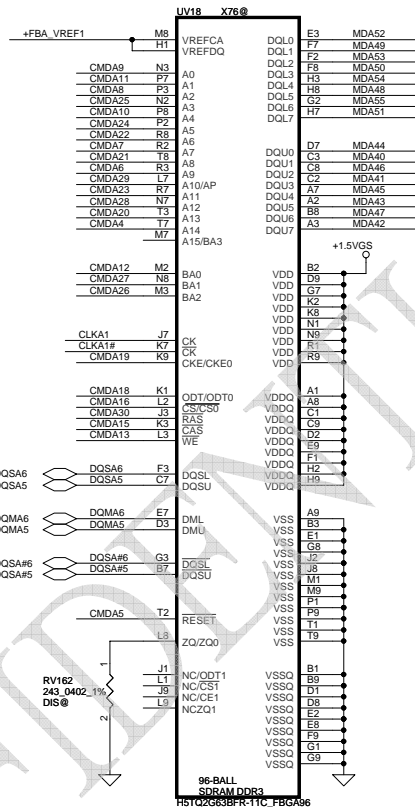
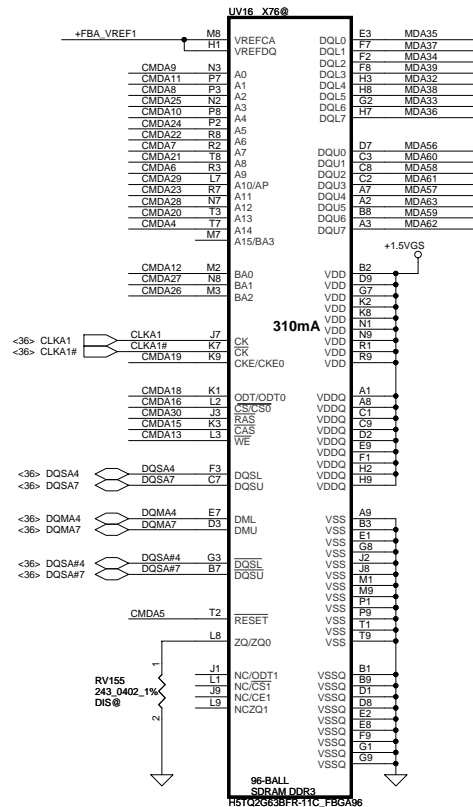
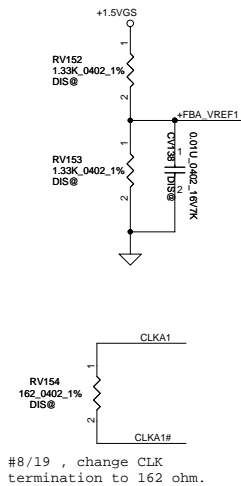


## Rank 0

## Data32~Data63

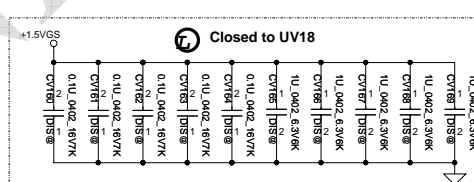
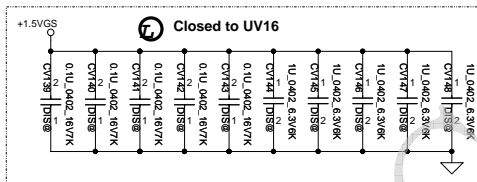
## Rank 0

MDA[0..63] <36,37>  
CMDA[90..0] <36,37>



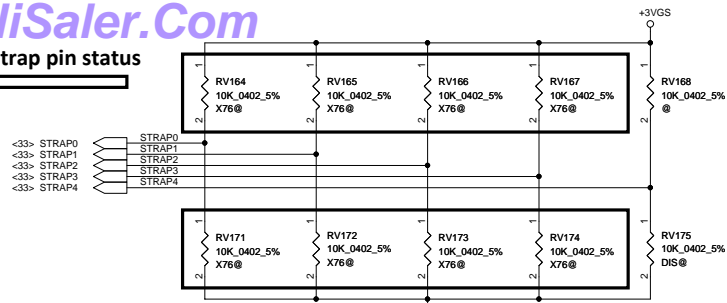
## Mode D Command Mapping

RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#	
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

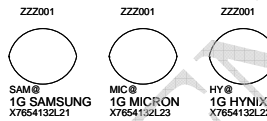
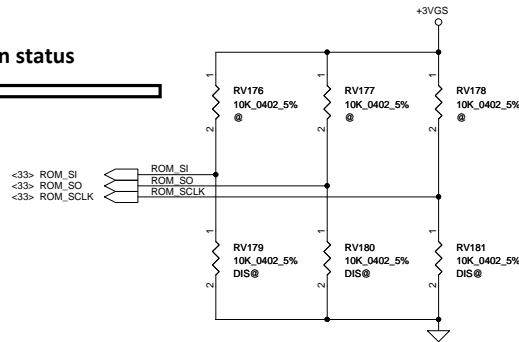


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				Rev	0.1

## Check Strap pin status



## Check SPI pin status



GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM CFG setup [3...0]	RAM CFG	R P/N
N15V-GM (23x23) 64bit (One CH single rank)	ZSO40	128M(X16)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00006H400	H5TC2G63FFR-11C 1000MHz	1100	RV171+RV172+RV167+RV166	
	ZSO50	128M(X16)	CHA	DDR3 Micron 128Mx16 1.5V	SA000067500	MT41J128M16JT-093G-K 1000MHz	0001	RV164+RV172+RV173+RV174	
		128M(X16)	CHA	DDR3 Samsung 128Mx16 1.5V	SA000068U40	K4W2G1646Q-BC1A 1000MHz	1110	RV165+RV166+RV167+RV171	

#9/5 RAM\_CFG follow RVL-06891-001 table 1.  
Dule Rank layout with single Rank population.

Table 123

Strap pin Name	Strap Mapping	Resistance	Polarity	Logical Strapping Bit0
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND.	
ROM_SI	SUB_VENDOR	10K	Pull-down to GND if no VBIOS ROM.	
ROM_SO	VGA_DEVICE	10K	Pull-down to GND(no diaplay).	
STRAP0	RAM_CFG[0]	10K		
STRAP1	RAM_CFG[1]	10K		
STRAP2	RAM_CFG[2]	10K		
STRAP3	RAM_CFG[3]	10K		
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND(PCIE Gen1).	

## SMBUS\_ALT\_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

## SUB\_VENDOR

0	Disable (Default)
1	

## VGA\_DEVICE

0	Non-Primary 3D Acceleration Device(Class Code 302h)(Default)
1	Primary Display or VGA Device .

## PCIE\_MAX\_SPEED

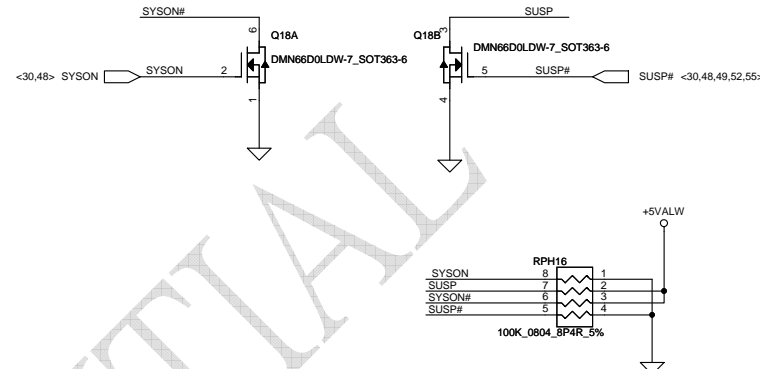
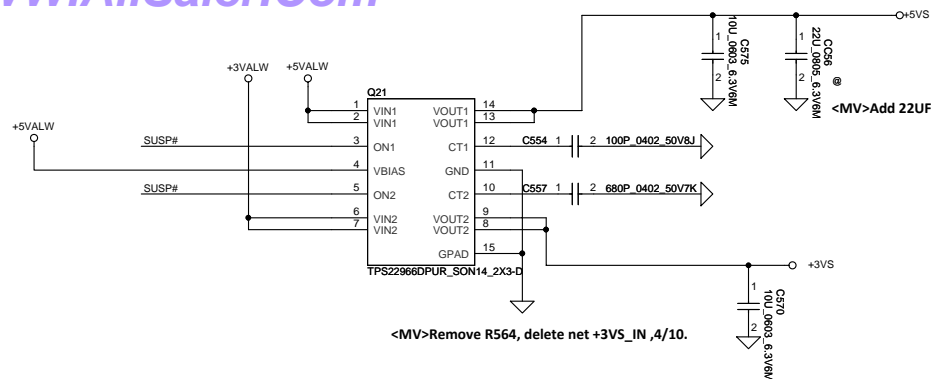
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

## USER Straps

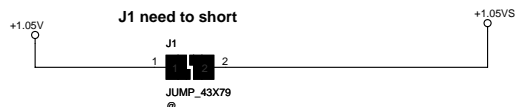
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1000-1100	Customer defined

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				Date: Thursday, March 20, 2014	Rev 1.0
				Sheet 39 of 54	

<MV>Remove R563, delete net +5VS\_IN\_4/10.

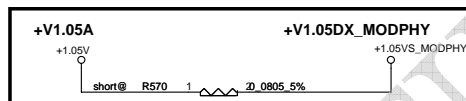


+1.05V TO +1.05VS



AO4430L  
VGS Max=+/- 20V  
VGS(Th) max=2.5V

Rds Max=5.5m @VGS=10V  
Rds Max=7.5m @VGS=4.5V

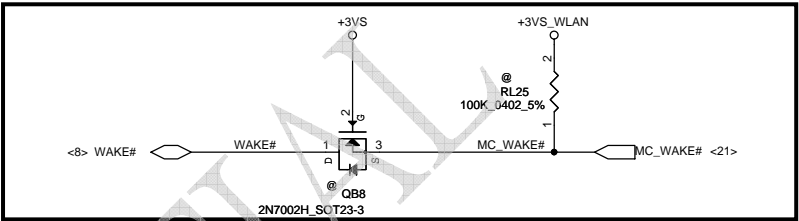


CPU +V1.05DX\_MODPHY  
Max Rds <6m ohm  
1840mA

AO4430L  
VGS Max=+/- 20V  
VGS(Th) max=2.5V  
Rds Max=5.5m @VGS=10V  
Rds Max=7.5m @VGS=4.5V

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						Date:		Thursday, March 20, 2014		Sheet		40 of 54	

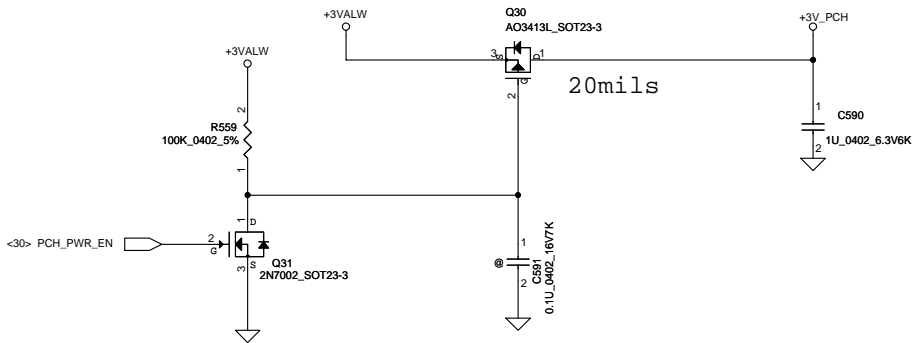
NGFF and WLAN



PV# 2013.01.23 Add QB8 abd RL25 to support OBFF  
PV# 2013.02.22 Unpop QB4 and RL23 for not support OBFF

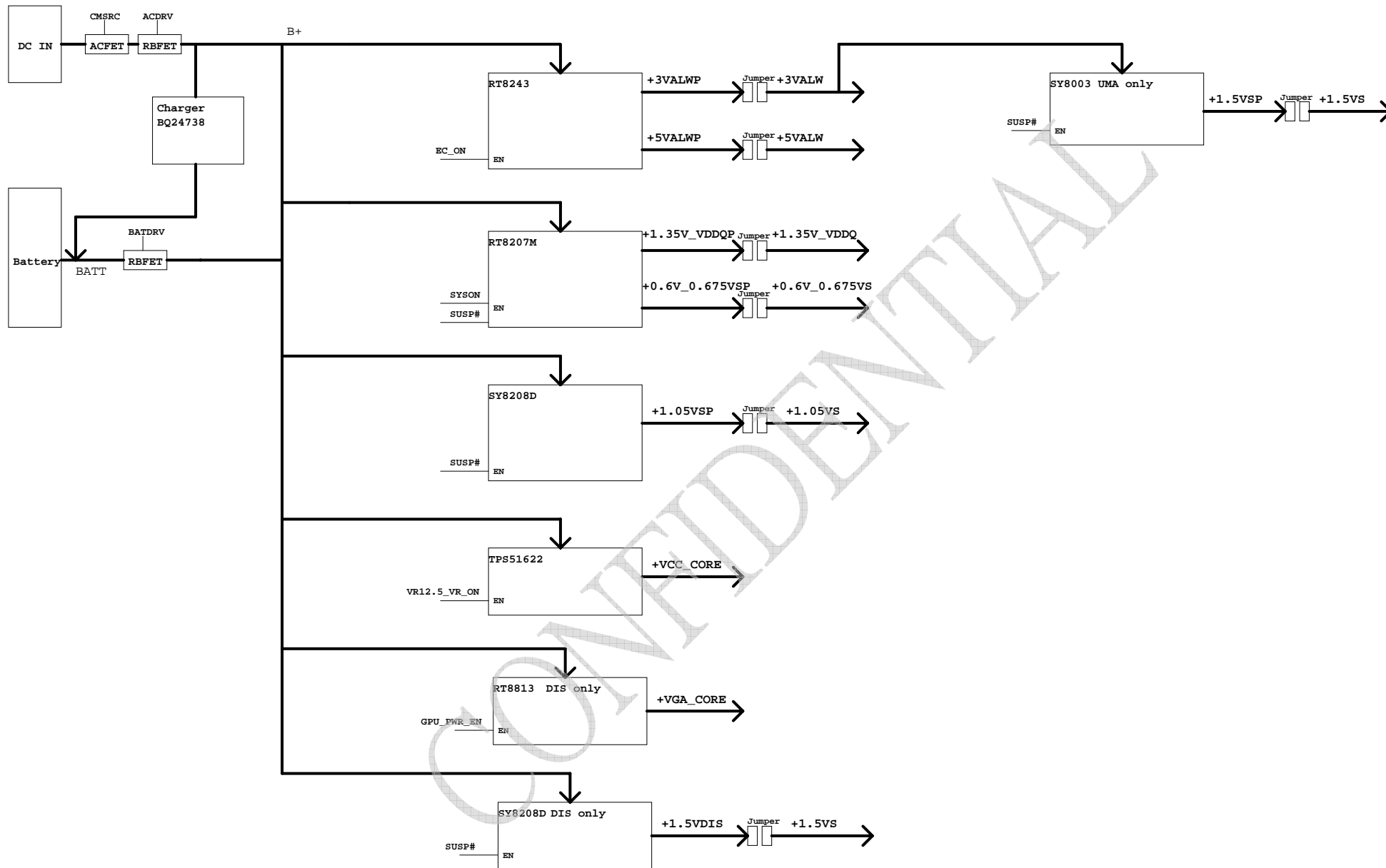
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		Date: Thursday, March 20, 2014		0.1	
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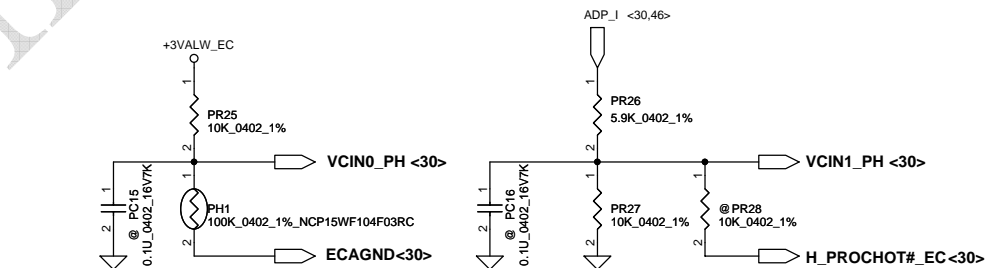
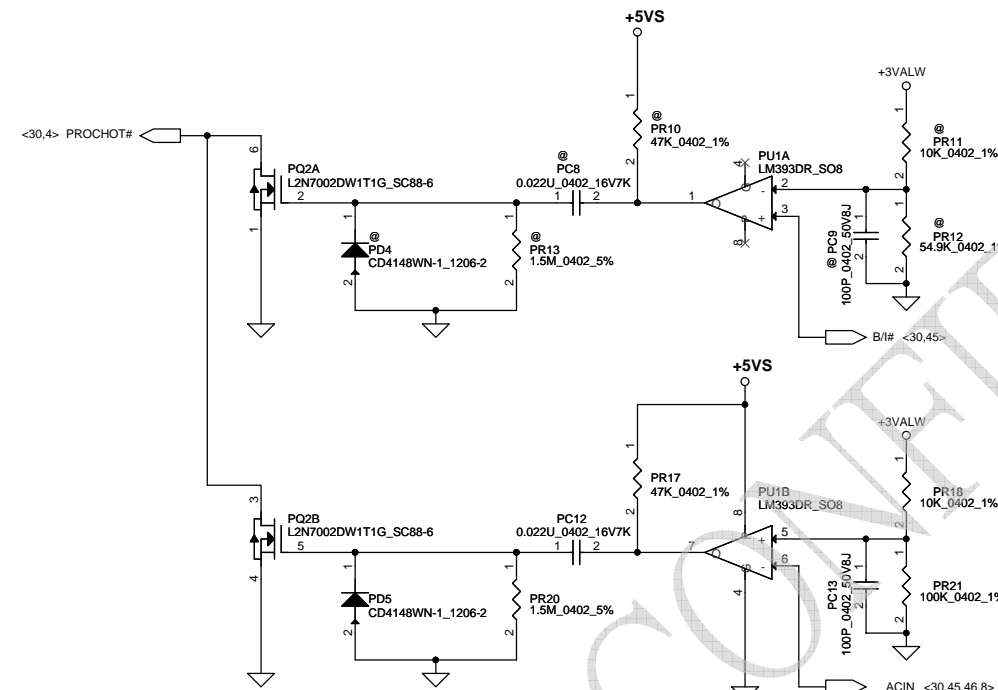
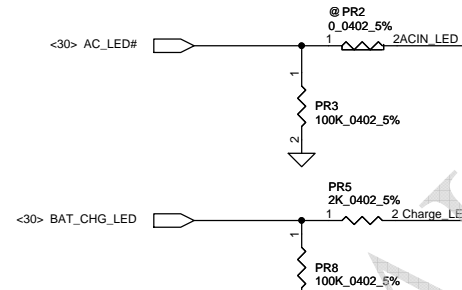
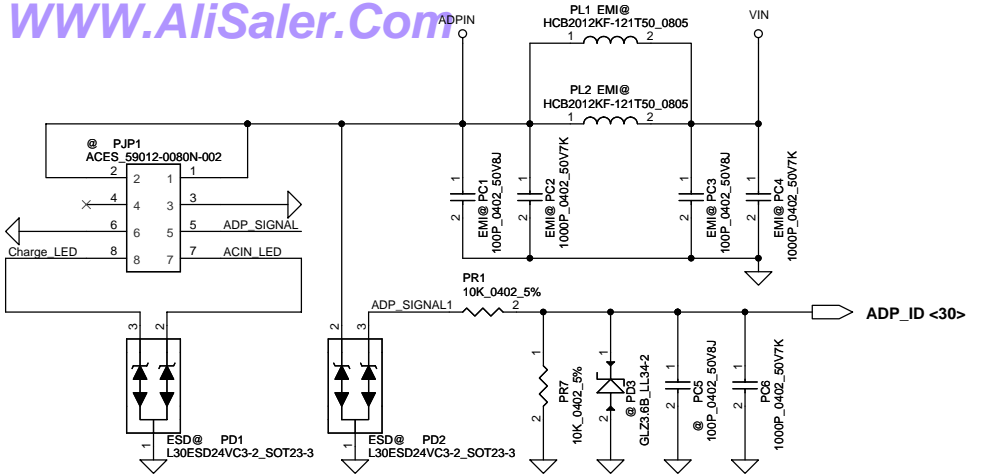


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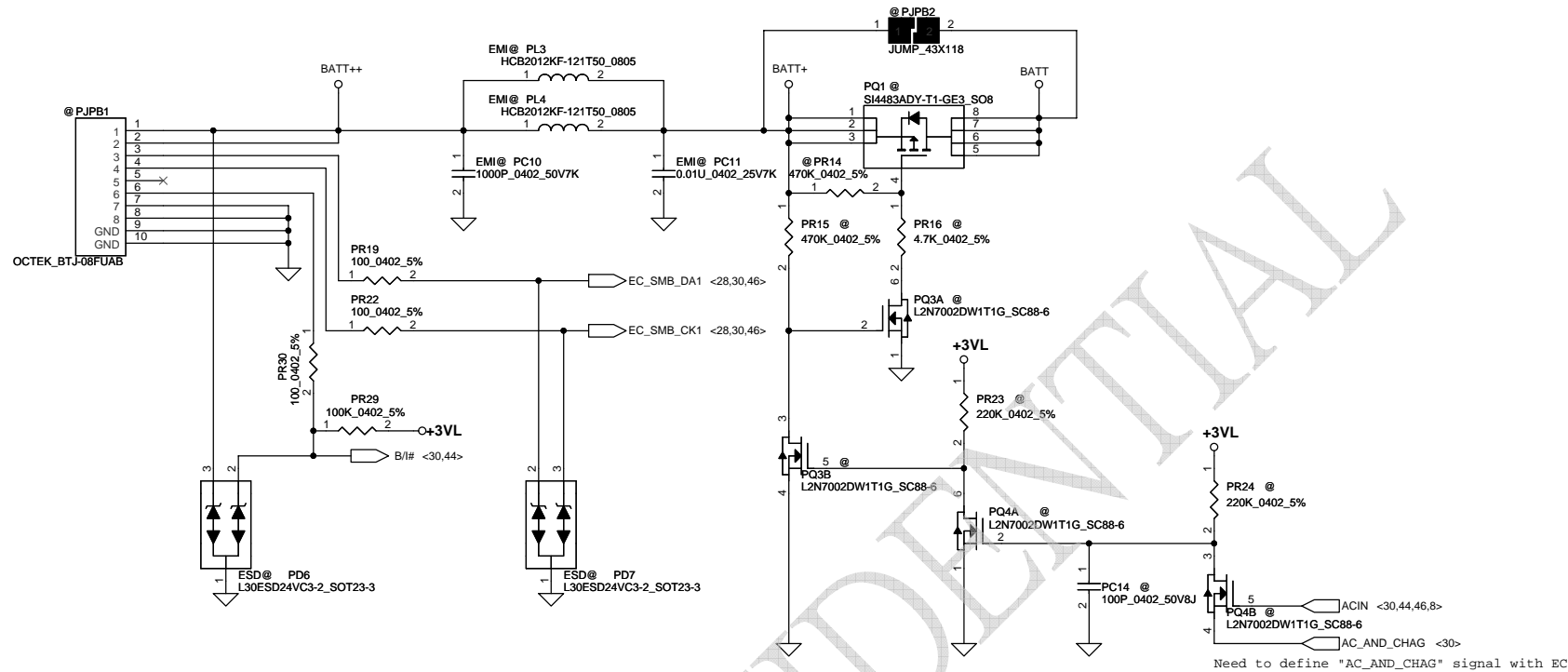
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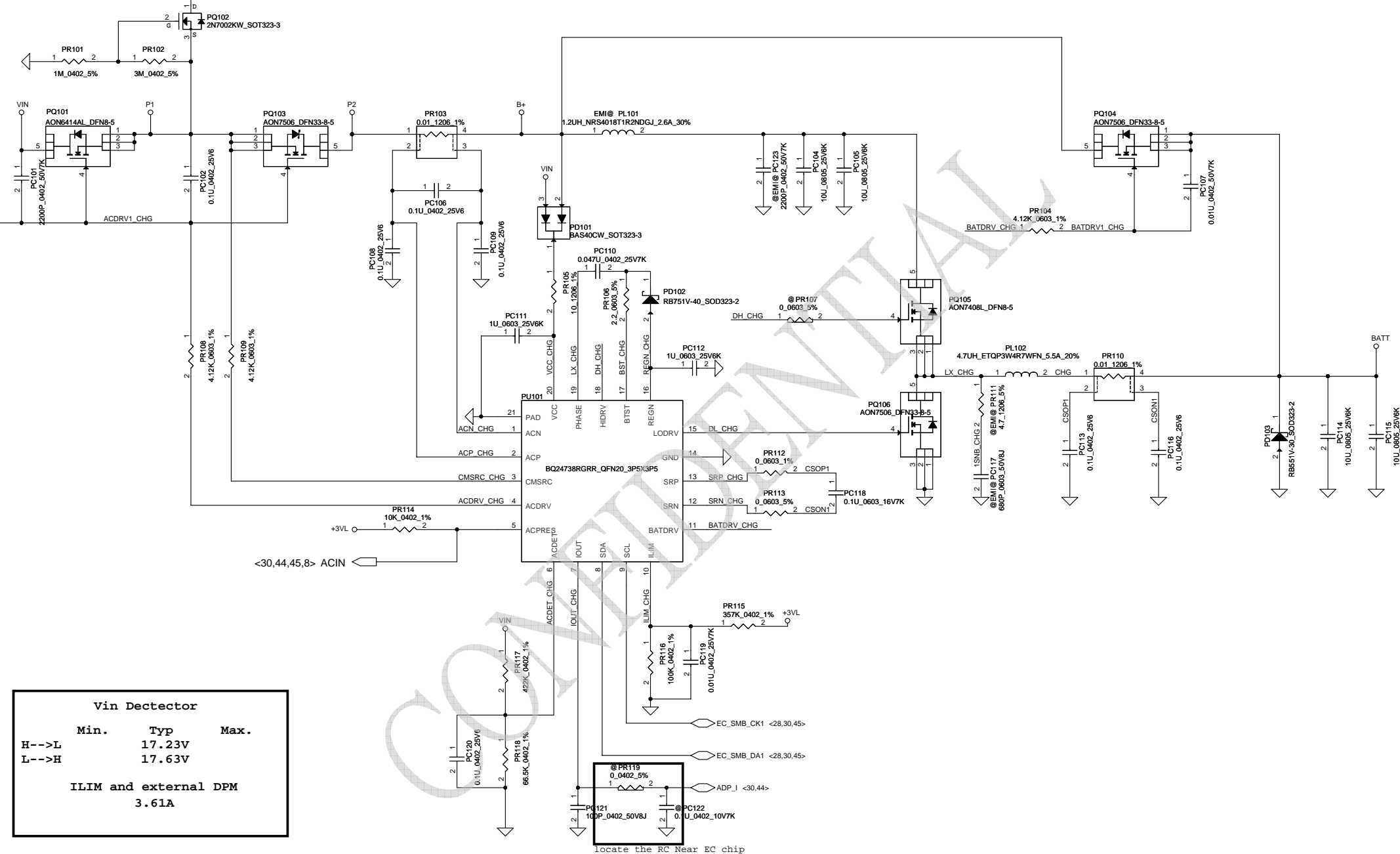
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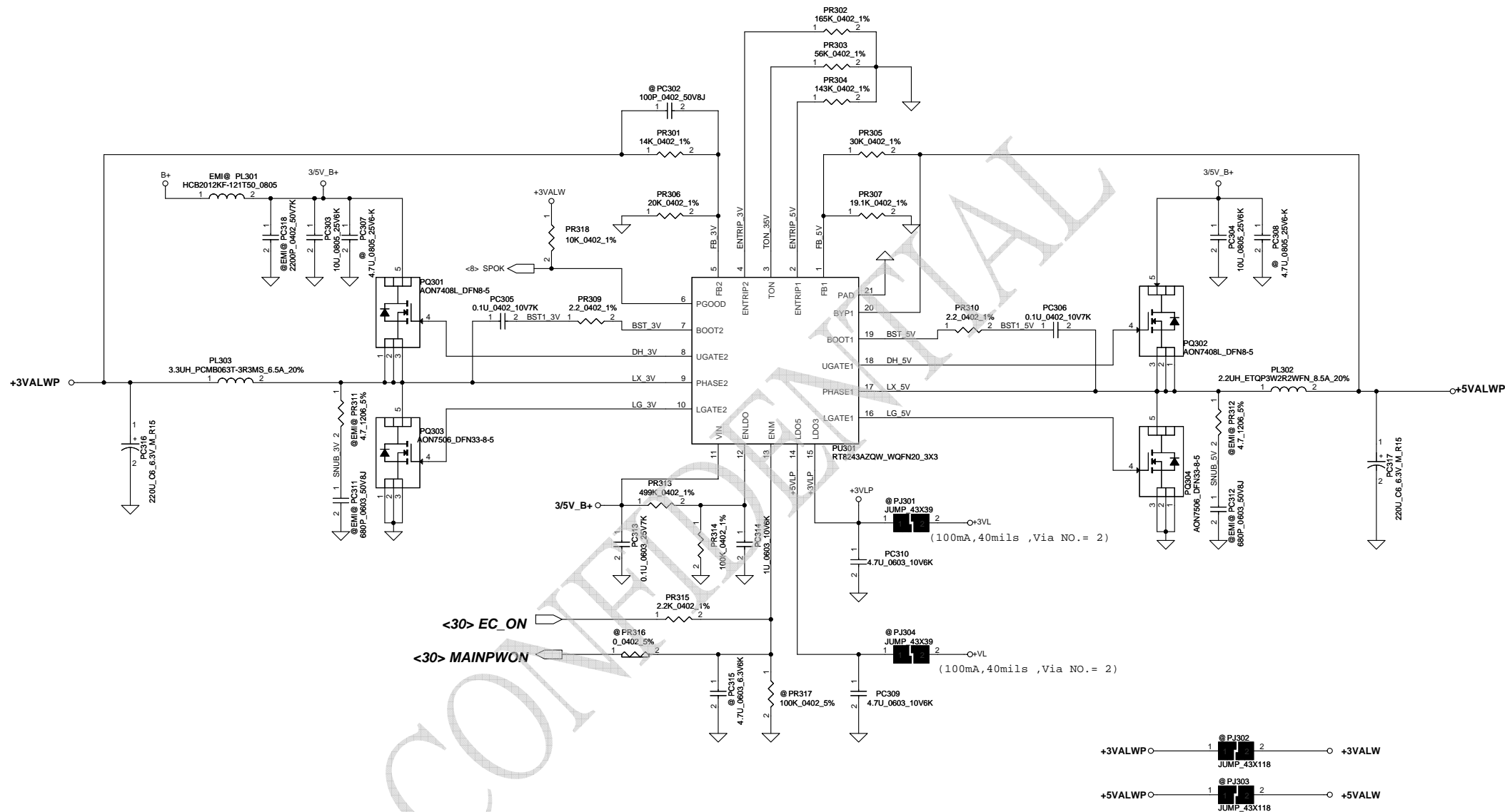
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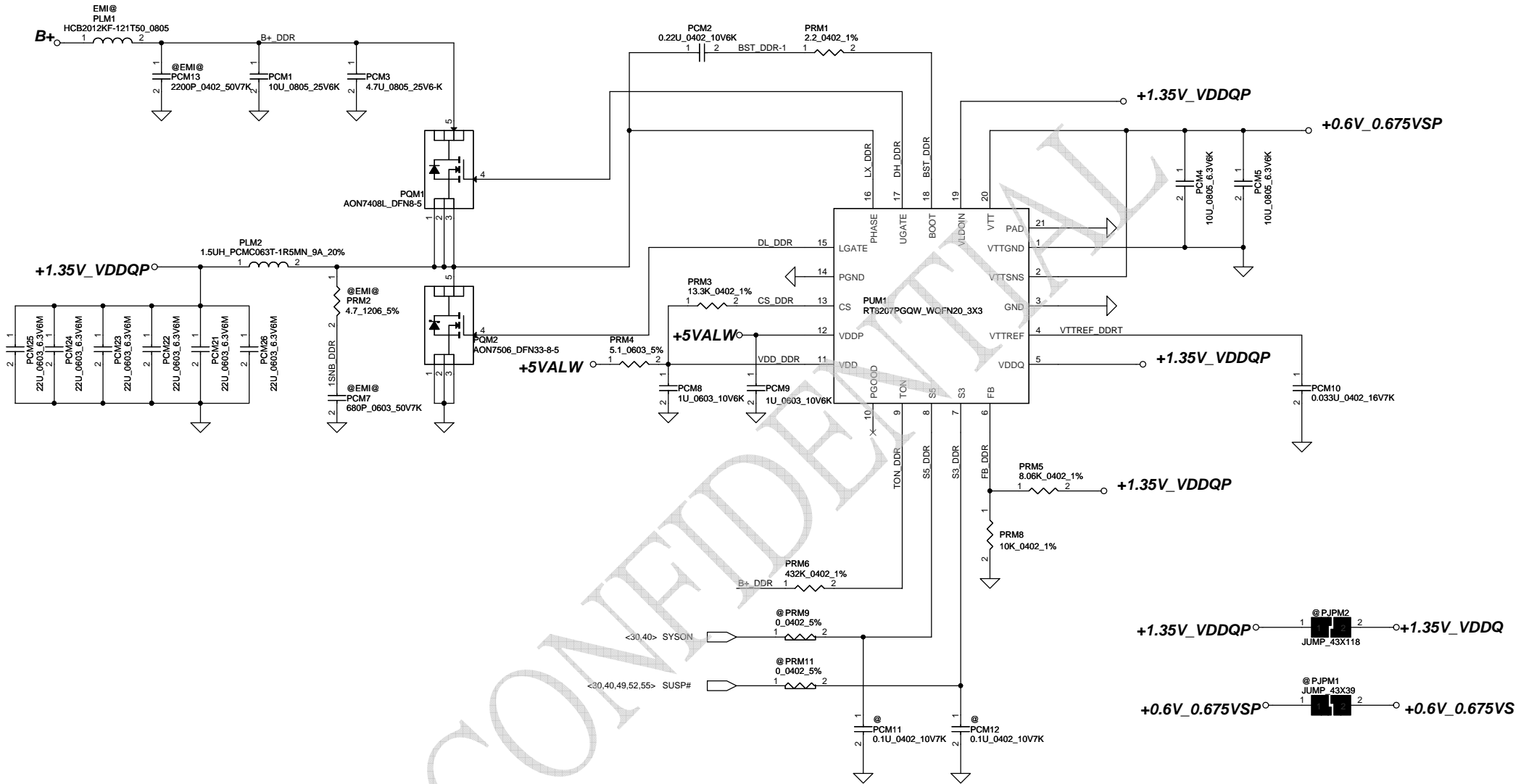
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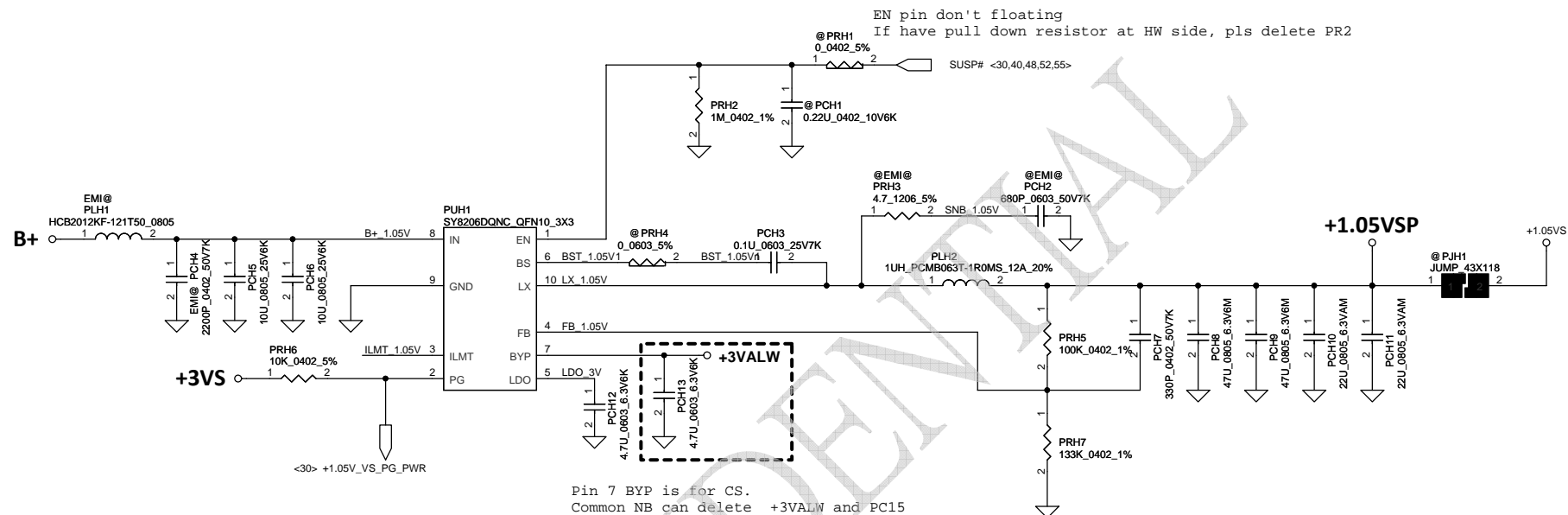
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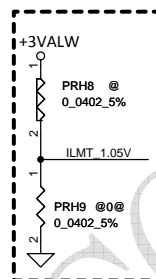
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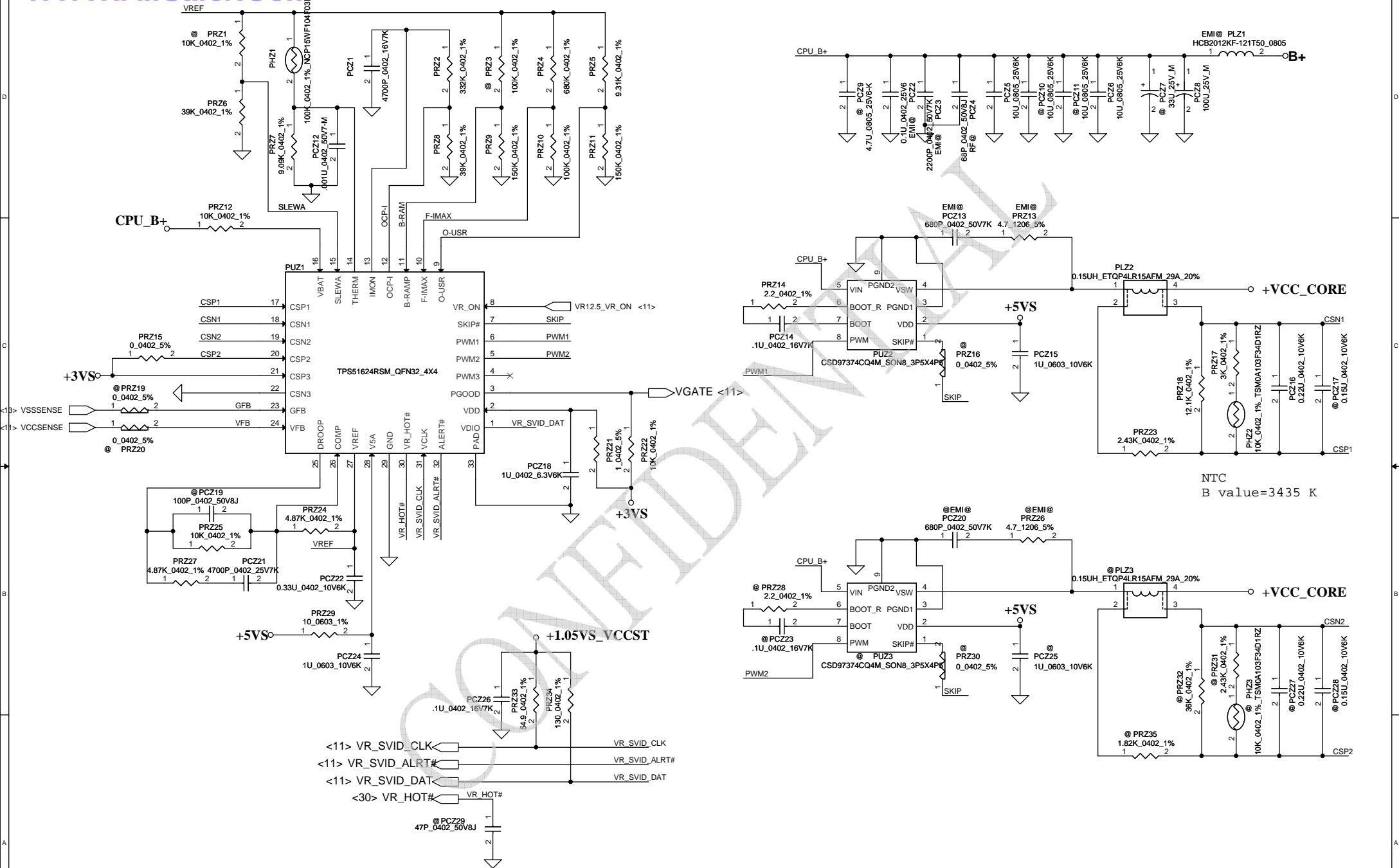


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peak 12A

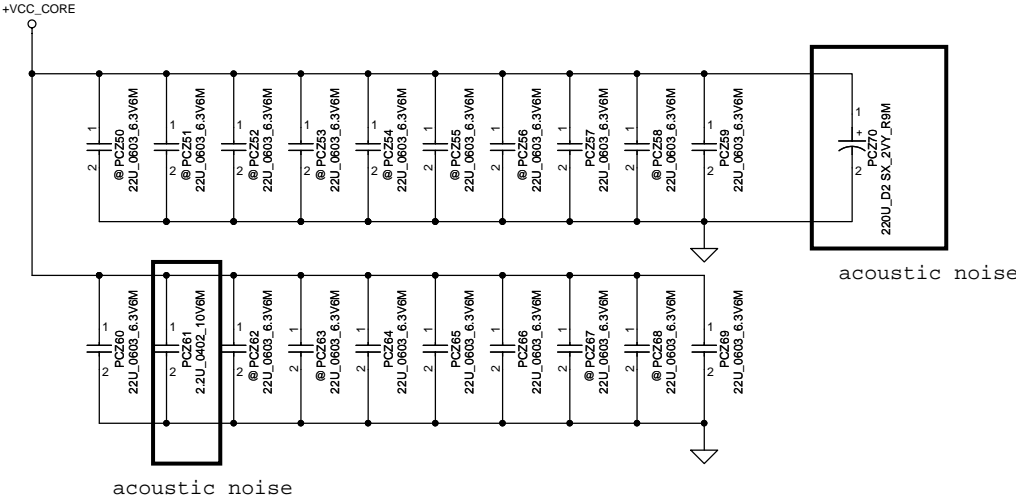


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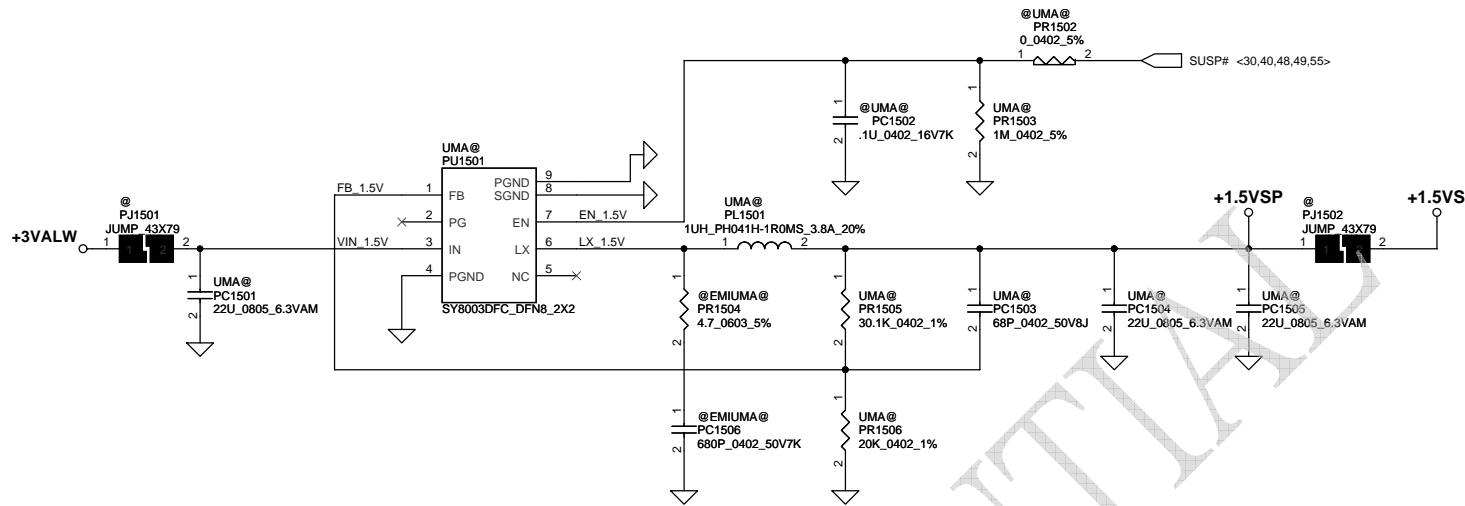
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				Date:	Thursday, March 20, 2014
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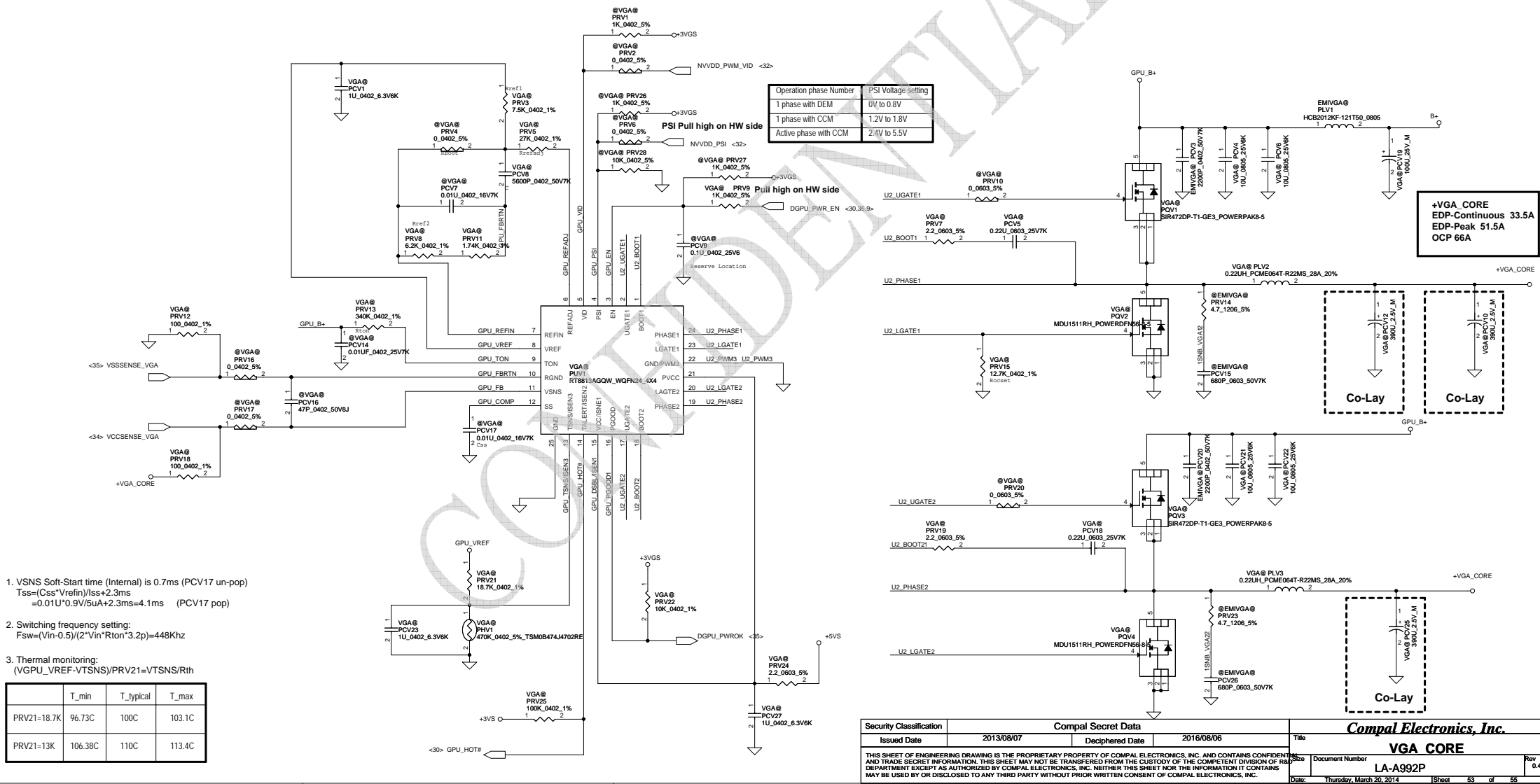


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Date: Thursday, March 20, 2014				Sheet	51 of 55

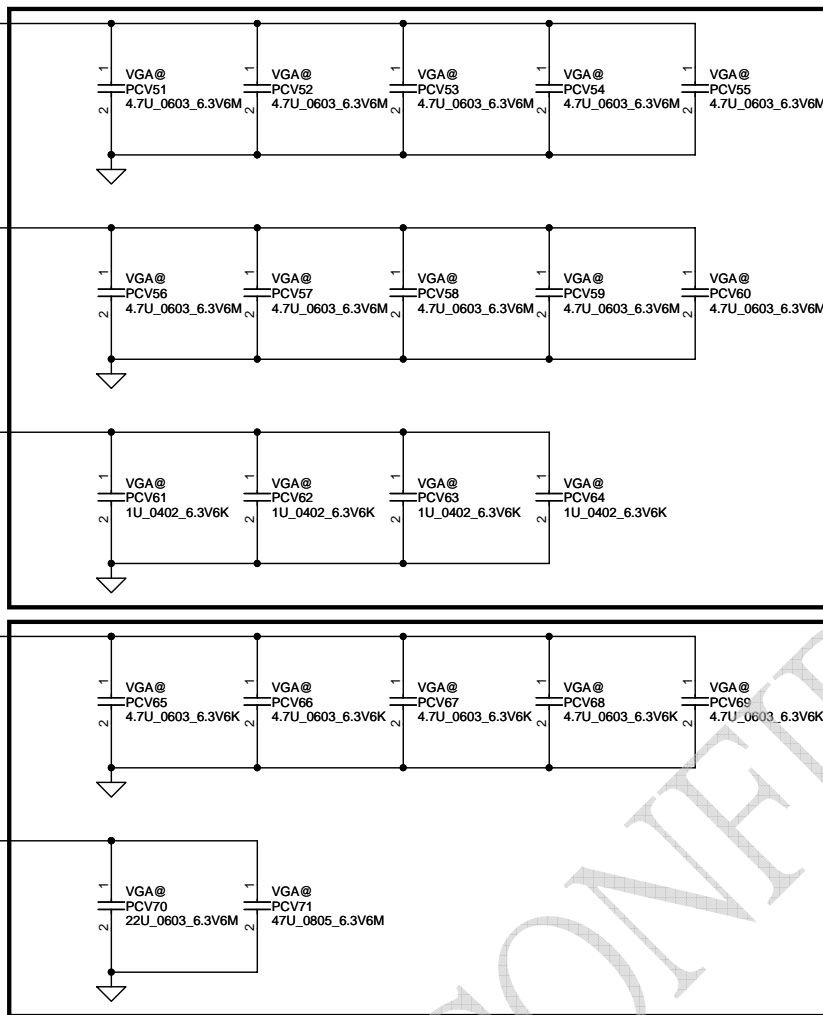


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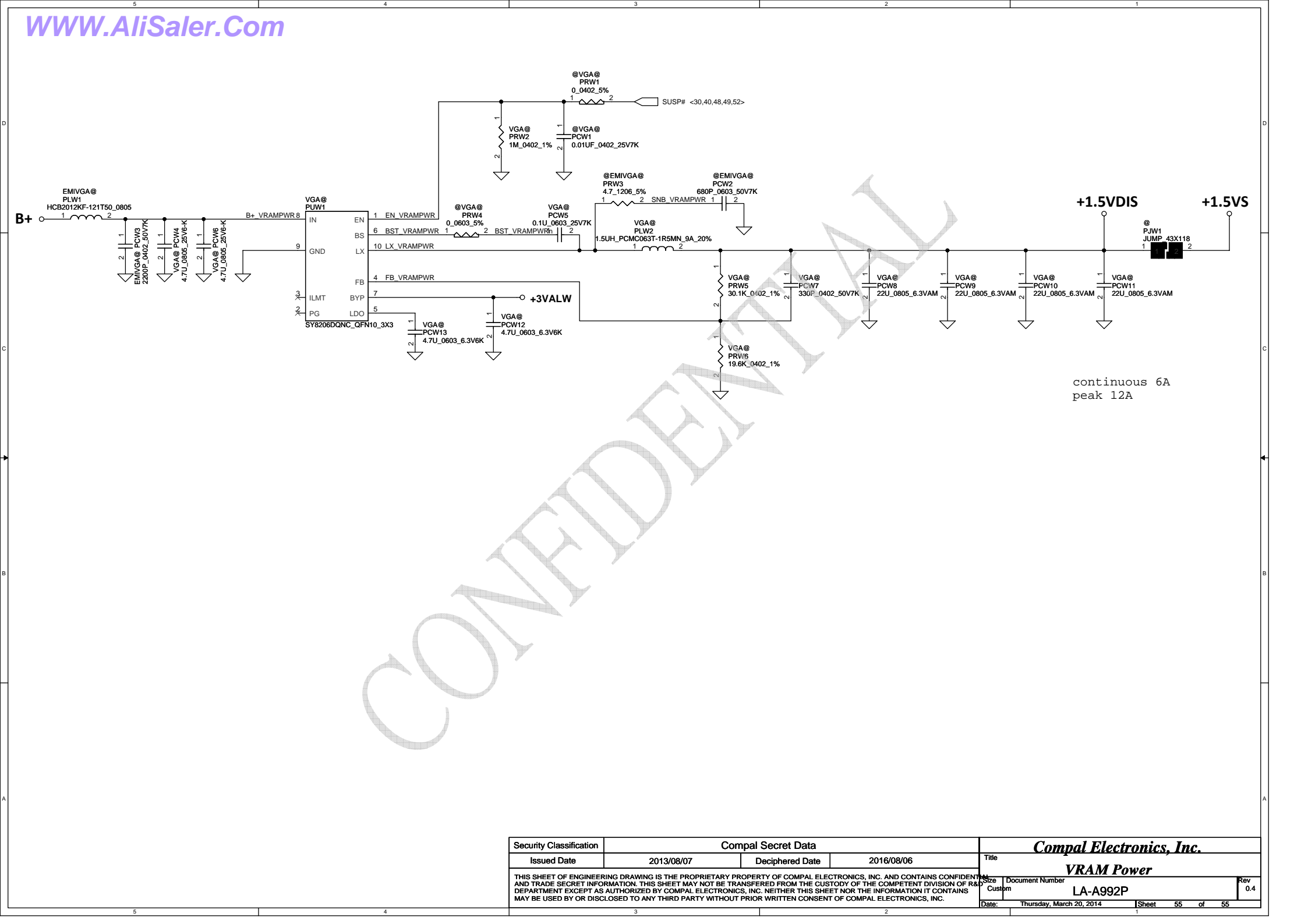
+VGA\_CORE



PLACE UNDER GPU

PLACE NEAR GPU

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continuous 6A  
peak 12A

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